TOSHIBA Multi-Chip Device

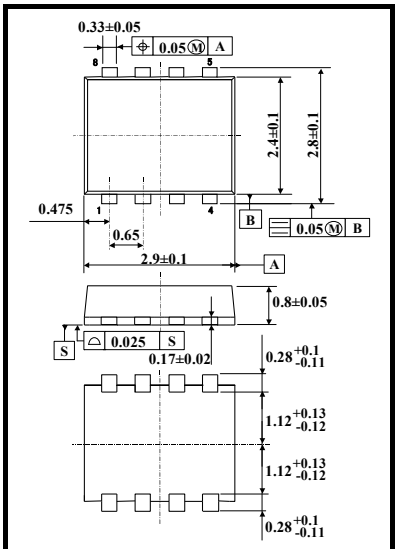
Transistor Silicon PNP Epitaxial Type／Field Effect Transistor Silicon P Channel MOS Type

# TPCP8G01

Unit: mm

## ○ Switching Applications

- Multi-chip discrete device: PNP Transistor and P Channel MOS FET
- Small footprint due to small and thin package




| | |
|---|---|
| JEDEC | ― |
| JEITA | ― |
| TOSHIBA | 2-3V1N |

Weight: 0.017 g (typ.)

## Absolute Maximum Ratings (Ta = 25°C)

### Transistor

| Characteristics | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Collector-base voltage | | $V_{CBO}$ | −30 | V |
| Collector-emitter voltage | | $V_{CEO}$ | −20 | V |
| Emitter-base voltage | | $V_{EBO}$ | −7 | V |
| Collector current (Note 1) | DC | $I_C$ | −3.0 | A |
| | Pulse | $I_{CP}$ | −5.0 | |
| Base current | | $I_B$ | −300 | mA |
| Collector power dissipation (Note 2) | DC | $P_C$ | 0.94 | W |
| | t = 10s | | 1.77 | |
| Junction temperature | | $T_j$ | 150 | °C |

### MOS FET

| Characteristics | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Drain-source voltage | | $V_{DSS}$ | −20 | V |
| Gate-source voltage | | $V_{GSS}$ | ±8 | V |
| Drain current (Note 1) | DC | $I_D$ | −2.0 | A |
| | Pulse | $I_{DP}$ | −4.0 | |
| Drain power dissipation (Note 1) | DC | $P_D$ (Note 1) | 0.94 | W |
| | t = 10s | | 1.77 | |
| Channel temperature | | $T_{ch}$ | 150 | °C |

## Common Absolute Maximum Ratings (Ta=25°C )

| Characteristics | Symbol | Rating | Unit |
|---|---|---|---|
| Storage temperature range | $T_{stg}$ | −55 to 150 | °C |

Note 1: Please use devices on condition that the junction temperature is below 150°C.

Note 2: Mounted on FR4 board (glass epoxy, 1.6 mm thick, Cu area: 645 $mm^2$)

Note 3: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

**Figure 1. Circuit configuration (top view)**

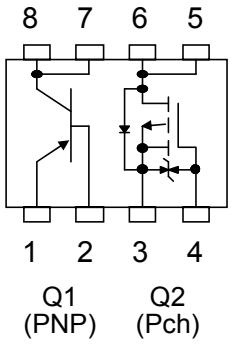
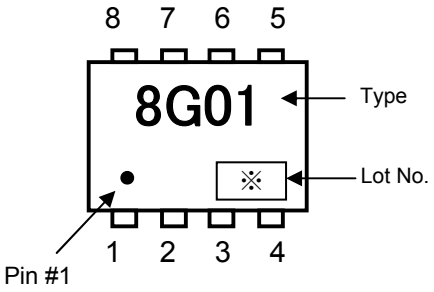



**Figure 2. Marking**

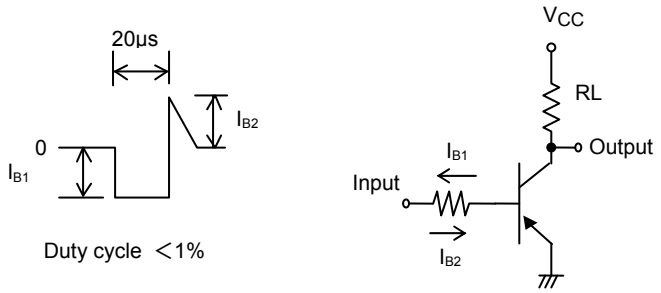


## Electrical Characteristics (Ta = 25°C)

### Transistor

| Characteristics | | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Collector cut-off current | | $I_{CBO}$ | $V_{CB}$ = −30 V, $I_E$ = 0 | — | — | −100 | nA |
| Emitter cut-off current | | $I_{EBO}$ | $V_{EB}$ = −7 V, $I_C$ = 0 | — | — | −100 | nA |
| Collector-emitter breakdown voltage | | $V_{(BR)\ CEO}$ | $I_C$ = −10 mA, $I_B$ = 0 | −20 | — | — | V |
| DC current gain | | $h_{FE}$ (1) | $V_{CE}$ = −2 V, $I_C$ = −0.5 A (Note4) | 200 | — | 500 | |
| | | $h_{FE}$ (2) | $V_{CE}$ = −2 V, $I_C$ = −1.6 A (Note4) | 100 | — | — | |
| Collector-emitter saturation voltage | | $V_{CE\ (sat)}$ | $I_C$ = −1.6 A, $I_B$ = −53 mA (Note4) | — | — | −0.19 | V |
| Base-emitter saturation voltage | | $V_{BE\ (sat)}$ | $I_C$ = −1.6 A, $I_B$ = −53 mA (Note4) | — | — | −1.10 | V |
| Collector output capacitance | | $C_{ob}$ | $V_{CB}$ = −10 V, $I_E$ = 0, f = 1MHz | — | 28 | — | pF |
| Switching time | Rise time | $t_r$ | See Figure 3 circuit diagram<br>$V_{CC}$ ≈ −12 V, $R_L$ = 7.5 Ω<br>$I_{B1}$ = 53 mA<br>$I_{B2}$ = 53 mA | — | 70 | — | ns |
| | Storage time | $t_{stg}$ | | — | 150 | — | |
| | Fall time | $t_f$ | | — | 40 | — | |

**Figure 3. Switching Time Test Circuit**



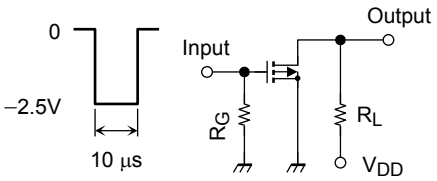

### MOS FET

| Characteristics | | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Drain-source breakdown voltage | | $V_{(BR)\ DSS}$ | $I_D$ = −1 mA, $V_{GS}$ = 0 | −20 | — | — | V |
| | | $V_{(BR)\ DSX}$ | $I_D$ = −1 mA, $V_{GS}$ = +8V | −12 | — | — | |
| Drain cut-off current | | $I_{DSS}$ | $V_{DS}$ = − 20 V, $V_{GS}$ = 0 | — | — | −10 | μA |
| Gate leakage current | | $I_{GSS}$ | $V_{GS}$ = ±8 V, $V_{DS}$ = 0 | — | — | ±1.0 | μA |
| Gate threshold voltage | | $V_{th}$ | $V_{DS}$ = −3 V, $I_D$ = −1 mA | −0.3 | — | −1.0 | V |
| Forward transfer admittance | | $\|Y_{fs}\|$ | $V_{DS}$ = −3 V, $I_D$ = −1 A (Note4) | 2.4 | 4.0 | — | S |
| Drain-source ON resistance | | $R_{DS(ON)}$ | $I_D$ = −1.0 A, $V_{GS}$ = −4 V (Note4) | — | 90 | 130 | mΩ |
| | | | $I_D$ = −0.5 A, $V_{GS}$ = −2.5 V (Note4) | — | 124 | 186 | |
| | | | $I_D$ = −0.2 A, $V_{GS}$ = −1.8V (Note4) | — | 180 | 320 | |
| Input capacitance | | $C_{iss}$ | $V_{DS}$ = −10 V, $V_{GS}$ = 0, f = 1 MHz | — | 335 | — | pF |
| Reverse transfer capacitance | | $C_{rss}$ | | — | 56 | — | |
| Output capacitance | | $C_{oss}$ | | — | 70 | — | |
| Switching time | Turn-on time | $t_{on}$ | See Figure 4 circuit diagram<br>$V_{DD}$ ≈ − 10V, $I_D$ = −1 A,<br>$V_{GS}$ = 0 to −2.5V, $R_G$ = 4.7Ω | — | 20 | — | ns |
| | Turn-off time | $t_{off}$ | | — | 20 | — | |
| Forward voltage (diode) | | $V_{DSF}$ | $I_D$ = 2 A , $V_{GS}$ = 0 (Note4) | — | 0.85 | 1.2 | V |

Note 4: Pulse test

**FIgure 4. Switching Time Test Curcuit**

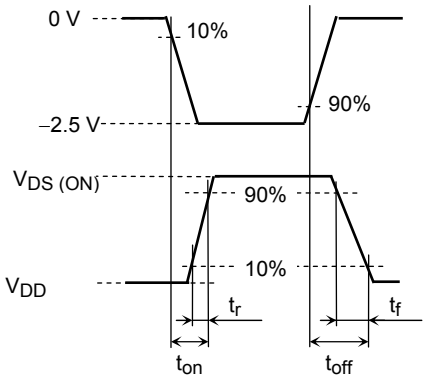
**(a) Test circuit**




$V_{DD}$ ≒ −10 V
$R_G$ = 4.7Ω
Duty cycle ≤ 1%
$V_{IN}$: $t_r$, $t_f$ < 5 ns
Common Source
Ta = 25°C

**(b) VIN**

**(c) VOUT**




## Precaution

$V_{th}$ can be expressed as the voltage between gate and source when the operating current value is low ($I_D$ = -mA for this product). For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than $V_{th}$ and $V_{GS\ (off)}$ requires a lower voltage than $V_{th}$. (The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$ .)

Take this into consideration when using the device.

## Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, ensure that the environment is protected Against electrostatic dischange. Operators should wear anti-static clothing, and containers and other objects that come Into direct contact with devices should be made of anti-static materials.

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