

NTD40N03R

Power MOSFET 40 Amps, 25 Volts

N-Channel DPAK

Features

- Planar HD3e Process for Fast Switching Performance
- Low $R_{DS(on)}$ to Minimize Conduction Loss
- Low C_{iss} to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High-Efficiency DC-DC Converters

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	25	Vdc
Gate-to-Source Voltage - Continuous	V_{GS}	± 20	Vdc
Thermal Resistance - Junction-to-Case	$R_{\theta JC}$	3.0	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	41.7	W
Drain Current			
- Continuous @ $T_A = 25^\circ\text{C}$, Chip	I_D	40	A
- Continuous @ $T_A = 25^\circ\text{C}$, Limited by Wires	I_D	32	A
- Single Pulse ($t_p \leq 10 \mu\text{s}$)	I_D	80	A
Thermal Resistance - Junction-to-Ambient (Note 1)	$R_{\theta JA}$	71.4	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.75	W
Drain Current - Continuous @ $T_A = 25^\circ\text{C}$	I_D	8.0	A
Thermal Resistance - Junction-to-Ambient (Note 2)	$R_{\theta JA}$	100	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.25	W
Drain Current - Continuous @ $T_A = 25^\circ\text{C}$	I_D	7.0	A
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

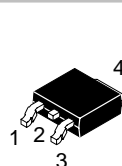
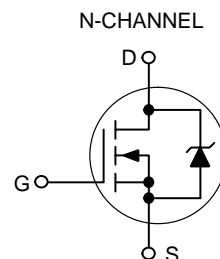
1. When surface mounted to an FR4 board using 0.5 sq in pad size.
2. When surface mounted to an FR4 board using minimum recommended pad size.



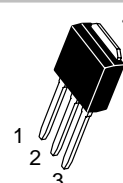
ON Semiconductor®

<http://onsemi.com>

40 AMPERES, 25 VOLTS
 $R_{DS(on)} = 12.6 \text{ m}\Omega$ (Typ)

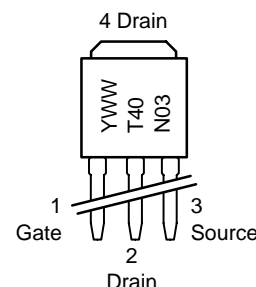
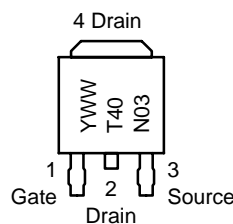


CASE 369C
DPAK
(Surface Mount)
STYLE 2



CASE 369D
DPAK
(Straight Lead)
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENTS



40N03 = Device Code
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
NTD40N03R	DPAK	75 Units/Rail
NTD40N03R-1	DPAK Straight Lead	75 Units/Rail
NTD40N03RT4	DPAK	2500 Tape & Reel

NTD40N03R

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Characteristics	Symbol	Min	Typ	Max	Unit
-----------------	--------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V _{GS} = 0 Vdc, I _D = 250 μAdc) Temperature Coefficient (Positive)	V _{(br)DSS}	25 -	28 -	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 20 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 20 Vdc, V _{GS} = 0 Vdc, T _J = 150°C)	I _{DSS}	- -	- -	1.0 10	μAdc
Gate-Body Leakage Current (V _{GS} = ±20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	-	-	±100	nAdc

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V _{DS} = V _{GS} , I _D = 250 μAdc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	1.0 -	1.7 -	2.0 -	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V _{GS} = 4.5 Vdc, I _D = 10 Adc) (V _{GS} = 10 Vdc, I _D = 10 Adc)	R _{DS(on)}	- -	18.6 12.6	23 16.5	mΩ
Forward Transconductance (Note 3) (V _{DS} = 10 Vdc, I _D = 10 Adc)	g _{FS}	-	20	-	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 20 Vdc, V _{GS} = 0 V, f = 1 MHz)	C _{iss}	-	584	-	pF
Output Capacitance		C _{oss}	-	254	-	
Transfer Capacitance		C _{rss}	-	99	-	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V _{GS} = 10 Vdc, V _{DD} = 10 Vdc, I _D = 10 Adc, R _G = 3 Ω)	t _{d(on)}	-	4.5	-	ns
Rise Time		t _r	-	19.5	-	
Turn-Off Delay Time		t _{d(off)}	-	16.7	-	
Fall Time		t _f	-	3.5	-	
Gate Charge	(V _{GS} = 4.5 Vdc, I _D = 10 Adc, V _{DS} = 10 Vdc) (Note 3)	Q _T	-	5.78	-	nC
		Q ₁	-	2.1	-	
		Q ₂	-	2.5	-	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = 10 Adc, V _{GS} = 0 Vdc) (Note 3) (I _S = 10 Adc, V _{GS} = 0 Vdc, T _J = 125°C)	V _{SD}	- -	0.85 0.71	1.2 -	Vdc
Reverse Recovery Time	(I _S = 10 Adc, V _{GS} = 0 Vdc, di _S /dt = 100 A/μs) (Note 3)	t _{rr}	-	20.4	-	ns
		t _a	-	8.25	-	
		t _b	-	12.1	-	
Reverse Recovery Stored Charge		Q _{RR}	-	0.007	-	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

NTD40N03R

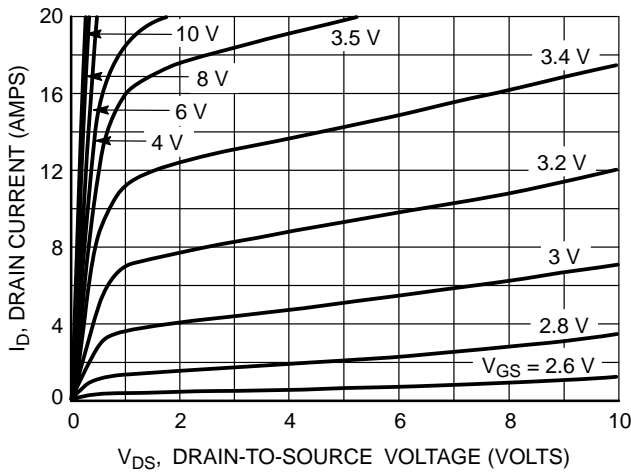


Figure 1. On-Region Characteristics

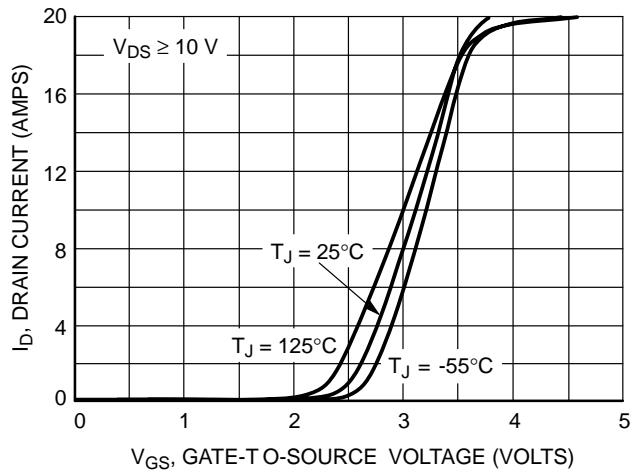


Figure 2. Transfer Characteristics

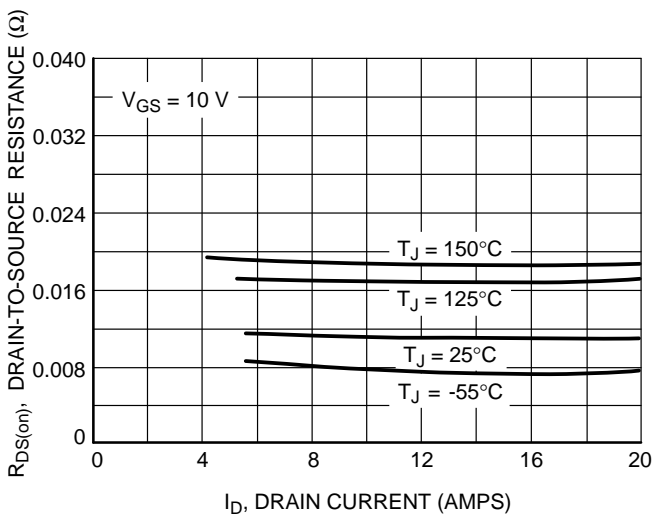


Figure 3. On-Resistance versus Drain Current and Temperature

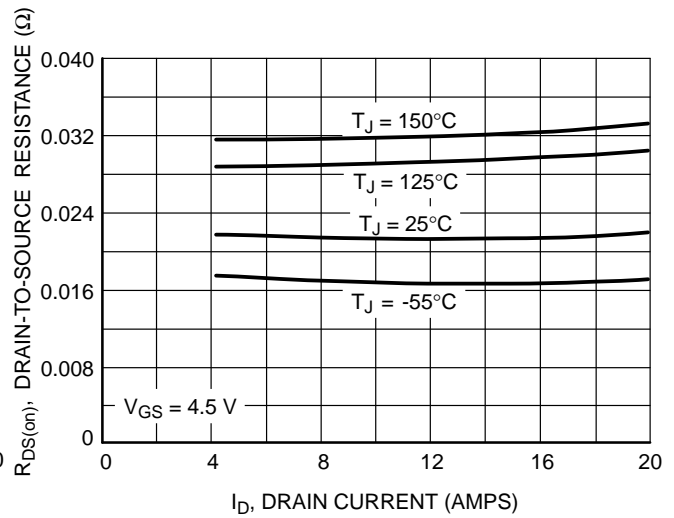


Figure 4. On-Resistance versus Drain Current and Temperature

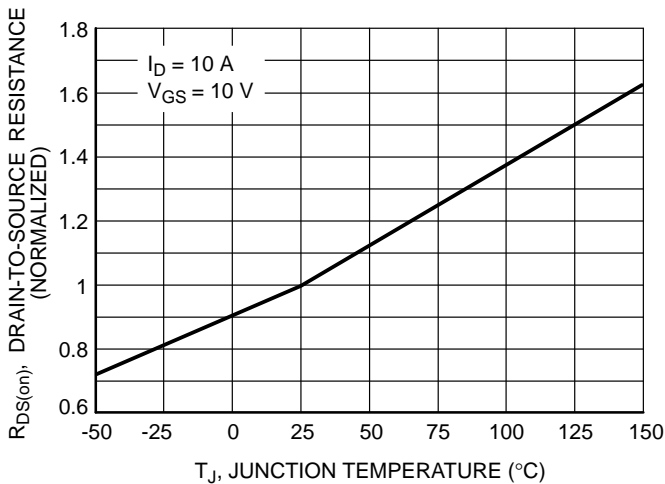


Figure 5. On-Resistance Variation with Temperature

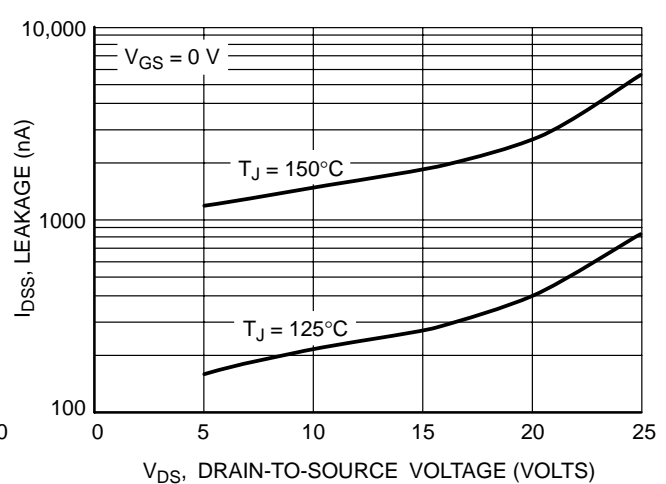


Figure 6. Drain-to-Source Leakage Current versus Voltage

NTD40N03R

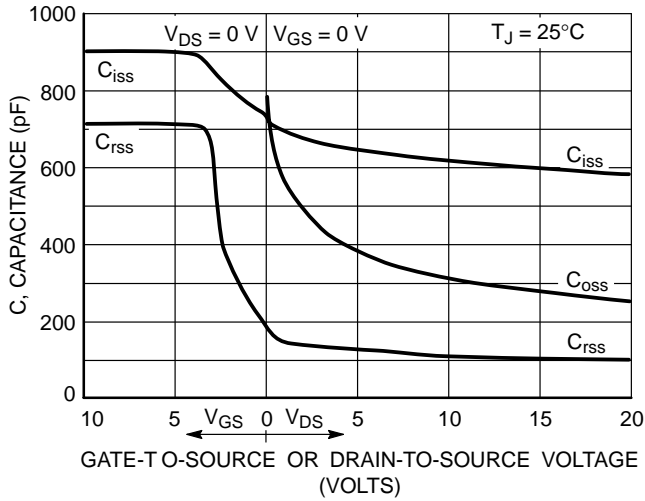


Figure 7. Capacitance Variation

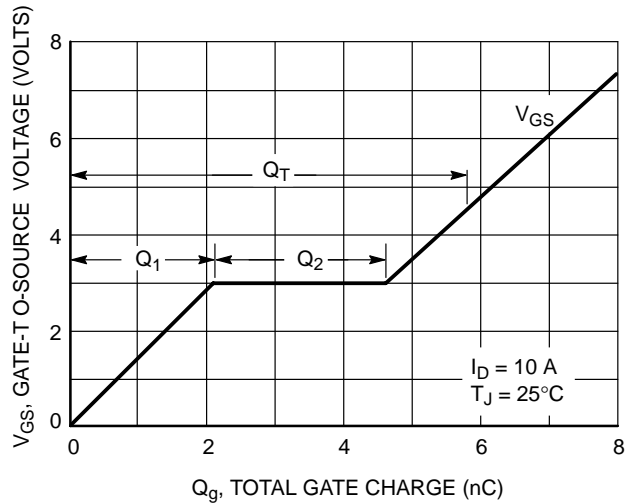


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

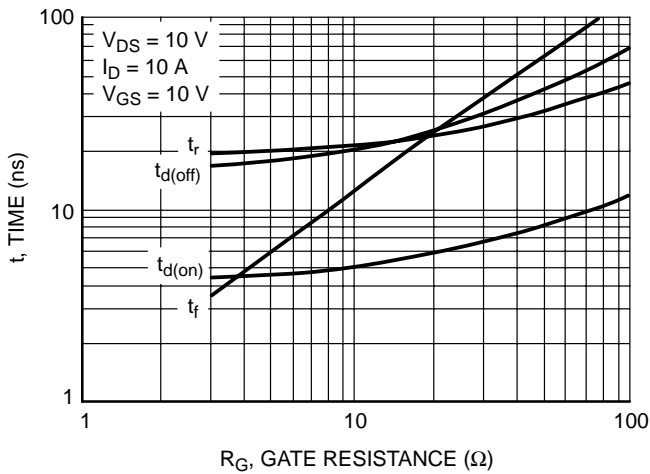


Figure 9. Resistive Switching Time Variation versus Gate Resistance

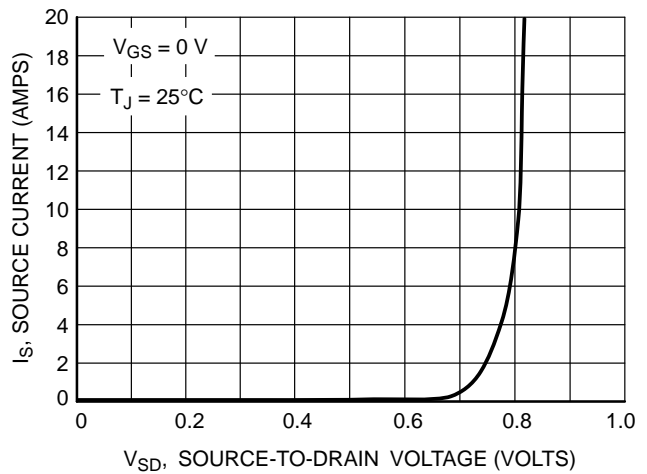


Figure 10. Diode Forward Voltage versus Current

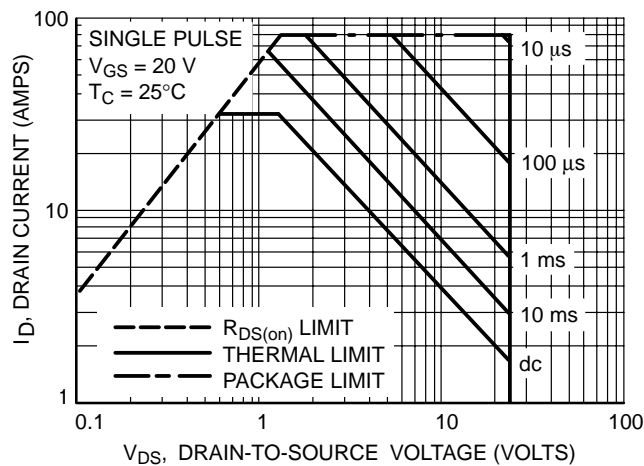


Figure 11. Maximum Rated Forward Biased Safe Operating Area

NTD40N03R

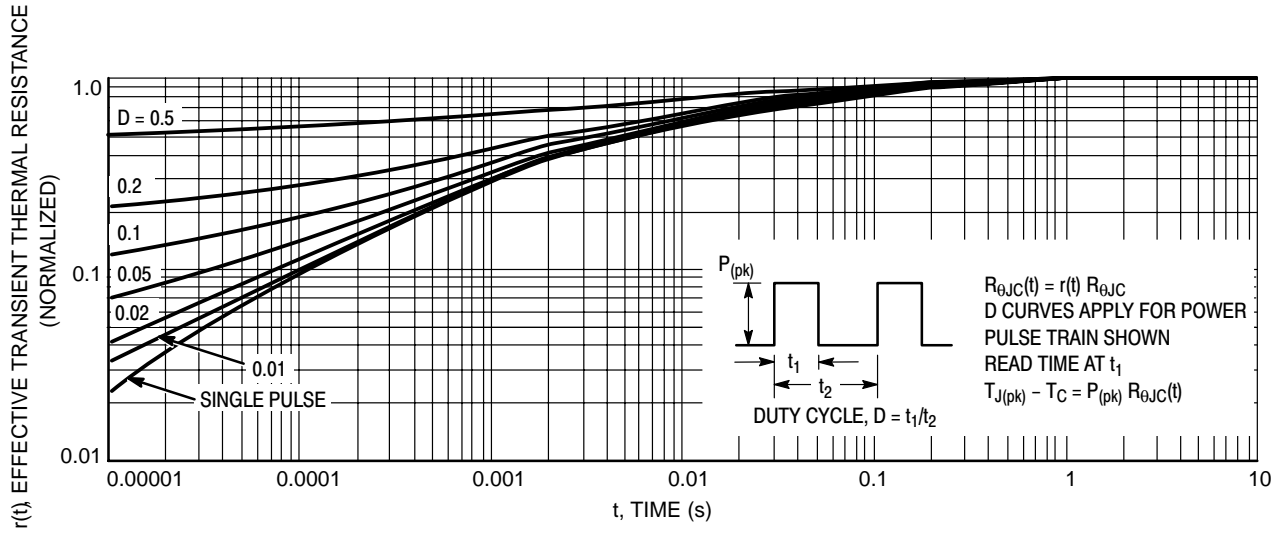


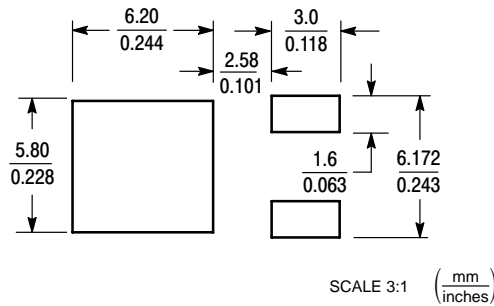
Figure 12. Thermal Response

NTD40N03R

RECOMMENDED FOOTPRINTS FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain/collector pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(\text{max})}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating ambient temperature, T_A . Using the values provided on the data sheet, P_D can be calculated as follows:

$$P_D = \frac{T_{J(\text{max})} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device. For a DPAK device, P_D is calculated as follows.

$$P_D = \frac{150^\circ\text{C} - 25^\circ\text{C}}{71.4^\circ\text{C/W}} = 1.75 \text{ Watts}$$

The 71.4°C/W for the DPAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 1.75 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 13.

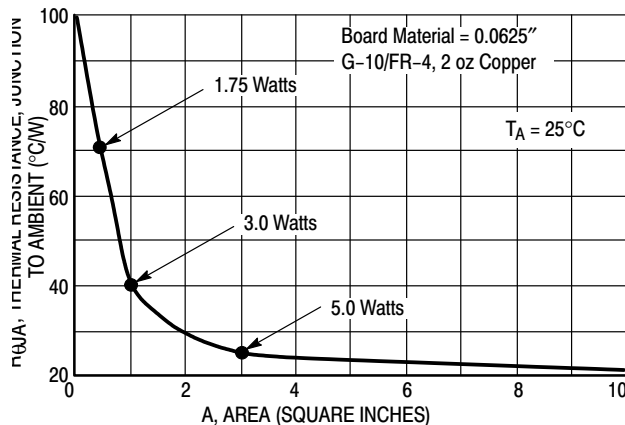
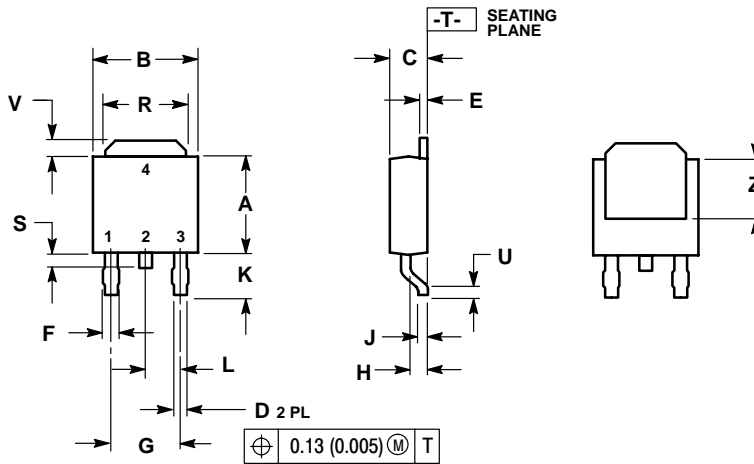


Figure 13. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)

NTD40N03R

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE) CASE 369C ISSUE O



- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

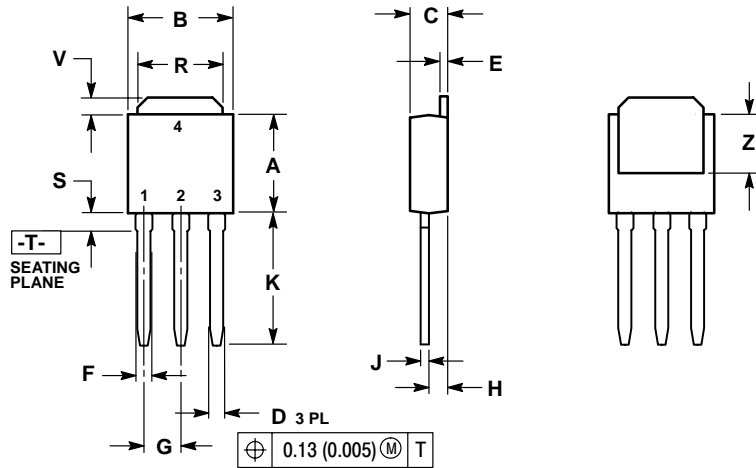
- STYLE 2:
 PIN 1. GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN

NTD40N03R

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE) CASE 369D ISSUE O

SCALE 1:1




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

JAPAN: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.