

PMN38EN

N-channel TrenchMOS logic level FET

Rev. 01 — 13 January 2006

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Logic level threshold
- Low threshold voltage
- Very fast switching
- Surface-mounted package

1.3 Applications

- Battery powered motor control
- High-speed switch in set top box power supplies
- Load switch in notebook computers
- Driver FET in DC-to-DC converters

1.4 Quick reference data

- $V_{DS} \leq 30 \text{ V}$
- $I_D \leq 5.4 \text{ A}$
- $R_{DSon} \leq 38 \text{ m}\Omega$
- $P_{tot} \leq 1.75 \text{ W}$

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 5, 6	drain (D)	<p>SOT457 (TSOP6)</p>	<p>mbb076 S</p>
3	gate (G)		
4	source (S)		

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3. Ordering information

Table 2: Ordering information

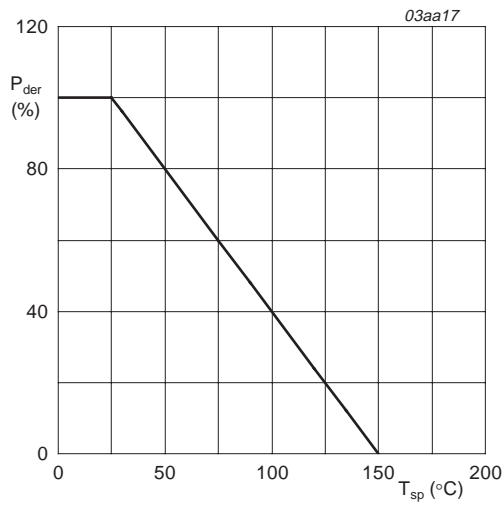
Type number	Package		
	Name	Description	Version
PMN38EN	TSOP6	plastic surface mounted package (TSOP6); 6 leads	SOT457

4. Limiting values

Table 3: Limiting values

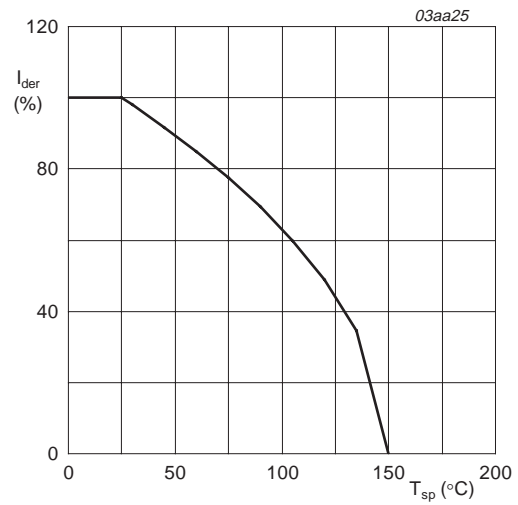
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	30	V
V_{GS}	gate-source voltage		-	± 20	V
I_D	drain current	$T_{sp} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 2 and 3	-	5.4	A
		$T_{sp} = 100\text{ °C}; V_{GS} = 10\text{ V};$ see Figure 2	-	3.4	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ see Figure 3	-	21.6	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C};$ see Figure 1	-	1.75	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source current	$T_{sp} = 25\text{ °C}$	-	1.45	A
I_{SM}	peak source current	$T_{sp} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	5.80	A



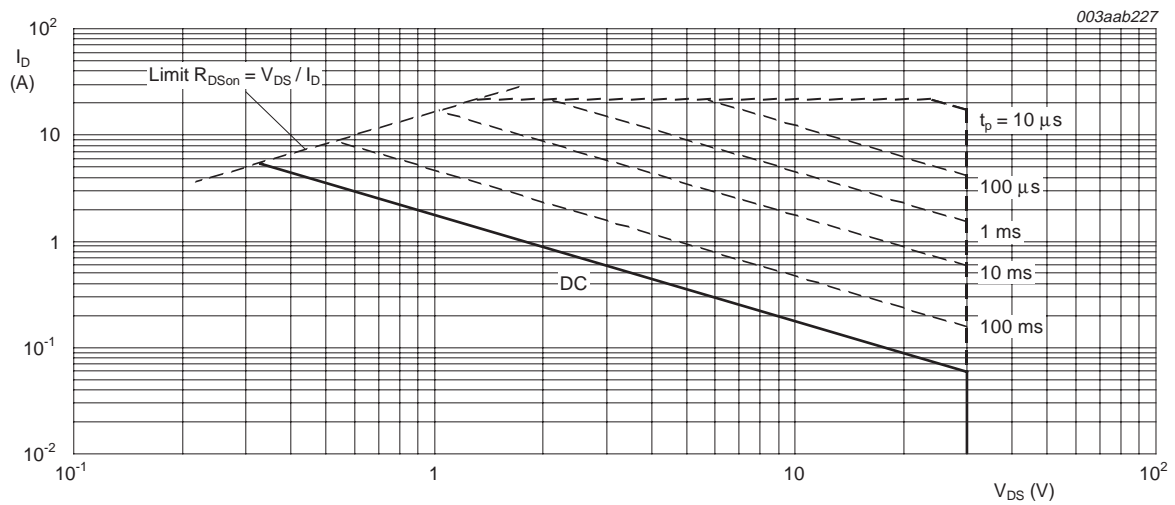
$$P_{der} = \frac{P_{tot}}{P_{tot(25\text{ }^{\circ}\text{C})}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature



$$I_{der} = \frac{I_D}{I_{D(25\text{ }^{\circ}\text{C})}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature



T_{sp} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 4	[1]	-	70	K/W

[1] Mounted on a metal clad board

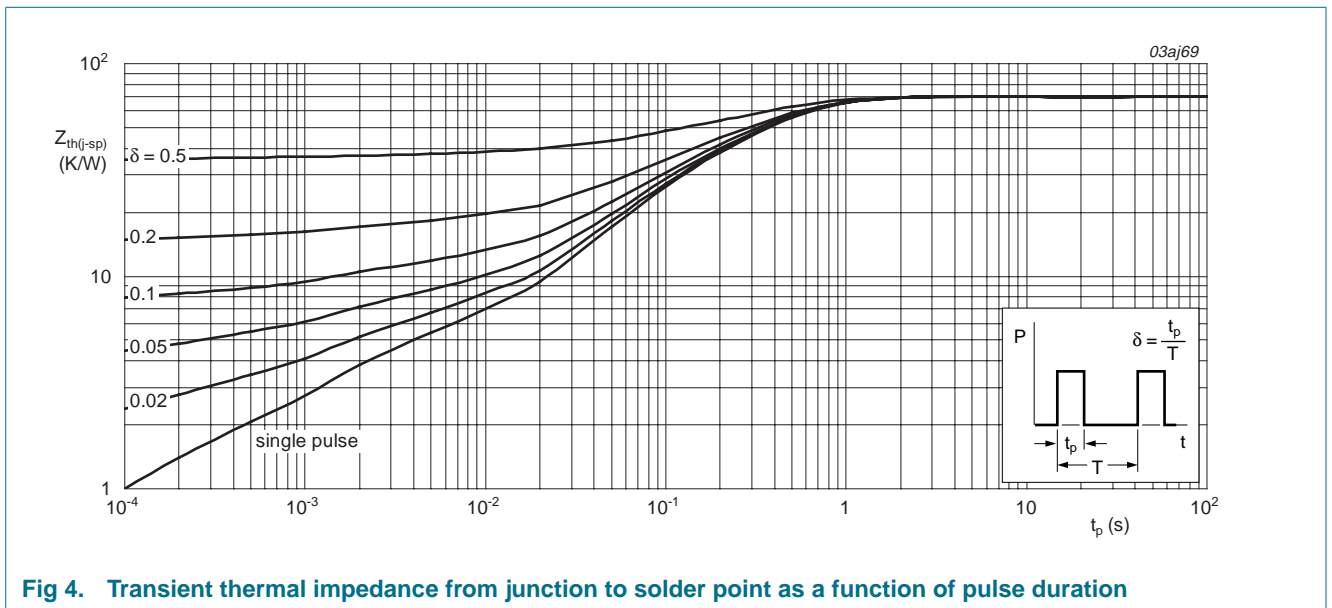


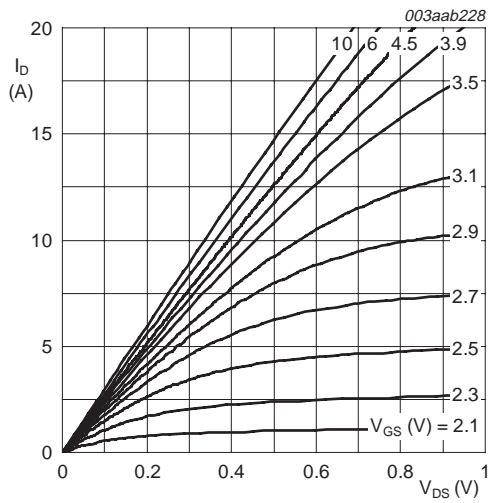
Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

Table 5: Characteristics

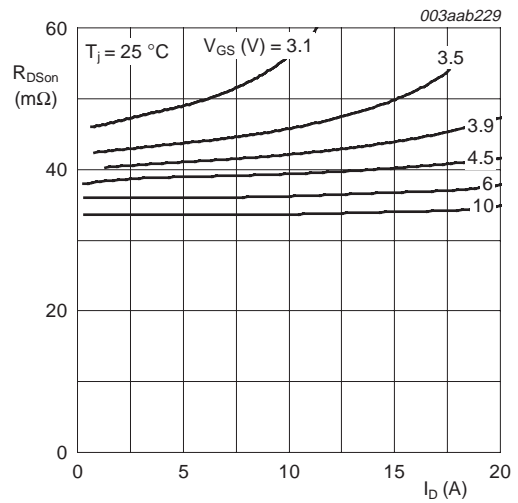
$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	30	-	-	V
		$T_j = -55\text{ °C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; see Figure 9 and 10				
		$T_j = 25\text{ °C}$	1	1.5	2	V
		$T_j = 150\text{ °C}$	0.6	-	-	V
		$T_j = -55\text{ °C}$	-	-	2.2	V
I_{DSS}	drain leakage current	$V_{DS} = 30\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ °C}$	-	0.01	1.0	μA
		$T_j = 150\text{ °C}$	-	-	10	μA
I_{GSS}	gate leakage current	$V_{GS} = \pm 20\text{ V}$; $V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 3\text{ A}$; see Figure 6 and 8				
		$T_j = 25\text{ °C}$	-	31	38	m Ω
		$T_j = 150\text{ °C}$	-	49.6	60.9	m Ω
		$V_{GS} = 4.5\text{ V}$; $I_D = 2.8\text{ A}$; see Figure 6 and 8	-	38	46	m Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 5\text{ A}$; $V_{DS} = 15\text{ V}$; $V_{GS} = 4.5\text{ V}$; see Figure 11 and 12	-	6.1	-	nC
Q_{GS}	gate-source charge		-	1.7	-	nC
Q_{GD}	gate-drain charge		-	2.35	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$; see Figure 14	-	495	-	pF
C_{oss}	output capacitance		-	100	-	pF
C_{rSS}	reverse transfer capacitance		-	70	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\text{ V}$; $R_L = 12\text{ }\Omega$; $V_{GS} = 4.5\text{ V}$; $R_G = 6\text{ }\Omega$	-	14	-	ns
t_r	rise time		-	19	-	ns
$t_{d(off)}$	turn-off delay time		-	28	-	ns
t_f	fall time		-	16	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 1.7\text{ A}$; $V_{GS} = 0\text{ V}$; see Figure 13	-	0.75	1.2	V



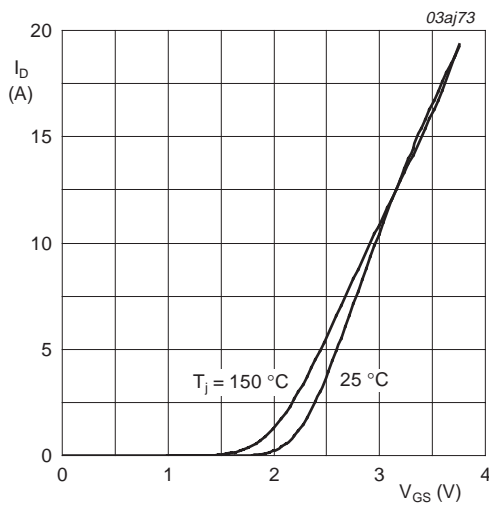
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



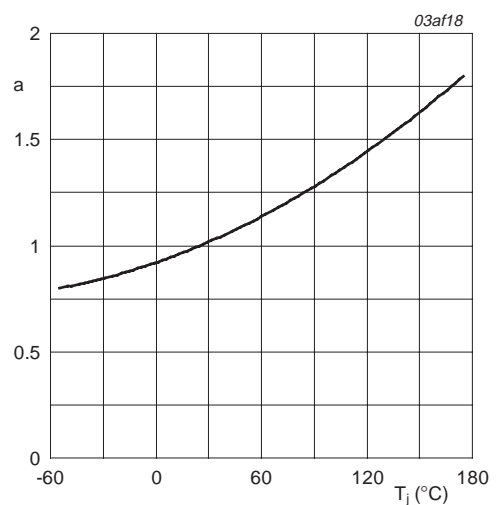
$T_j = 25\text{ }^\circ\text{C}$

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



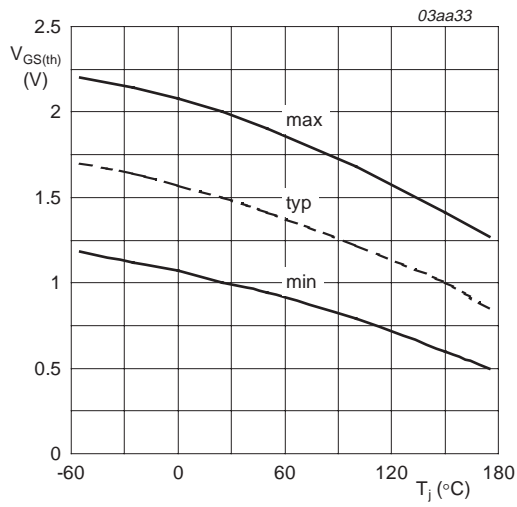
$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DS(on)}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



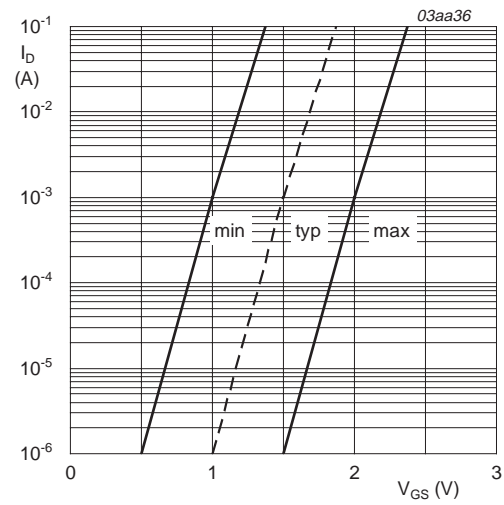
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25\text{ }^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



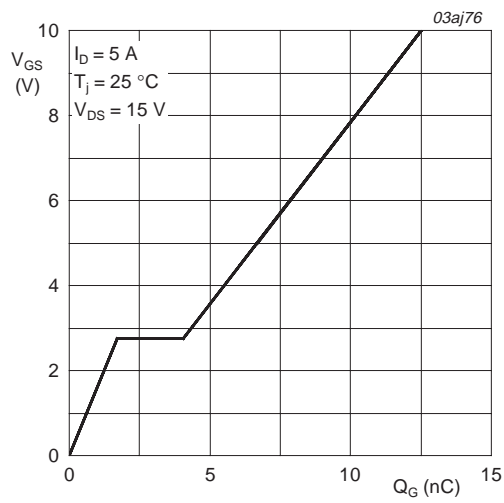
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



$T_j = 25 \text{ }^{\circ}C; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage



$I_D = 5 \text{ A}; V_{DS} = 15 \text{ V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values

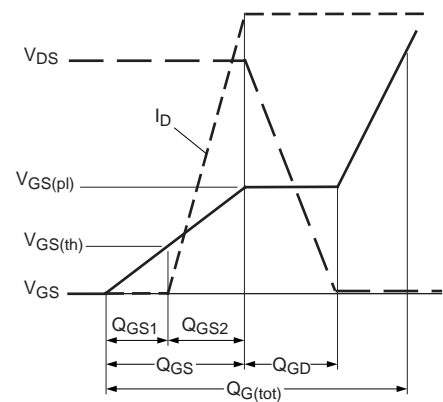
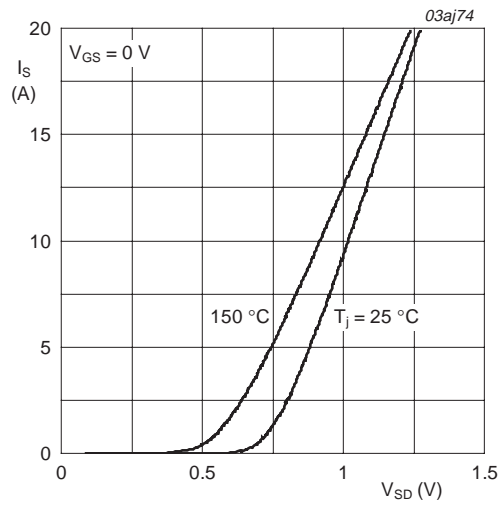
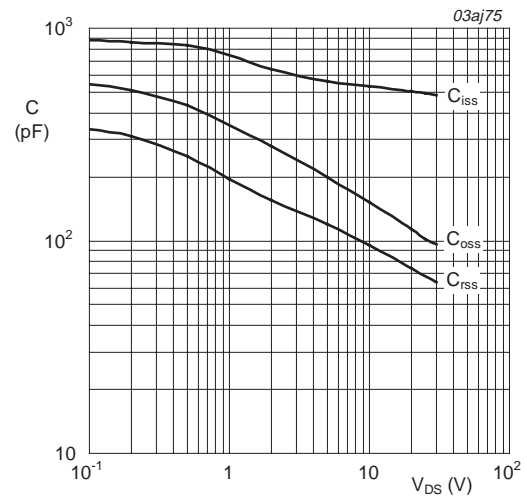


Fig 12. Gate charge waveform definitions



$T_j = 25 \text{ °C}$ and 150 °C ; $V_{GS} = 0 \text{ V}$

Fig 13. Source current as a function of source-drain voltage; typical values



$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic surface mounted package (TSOP6); 6 leads

SOT457

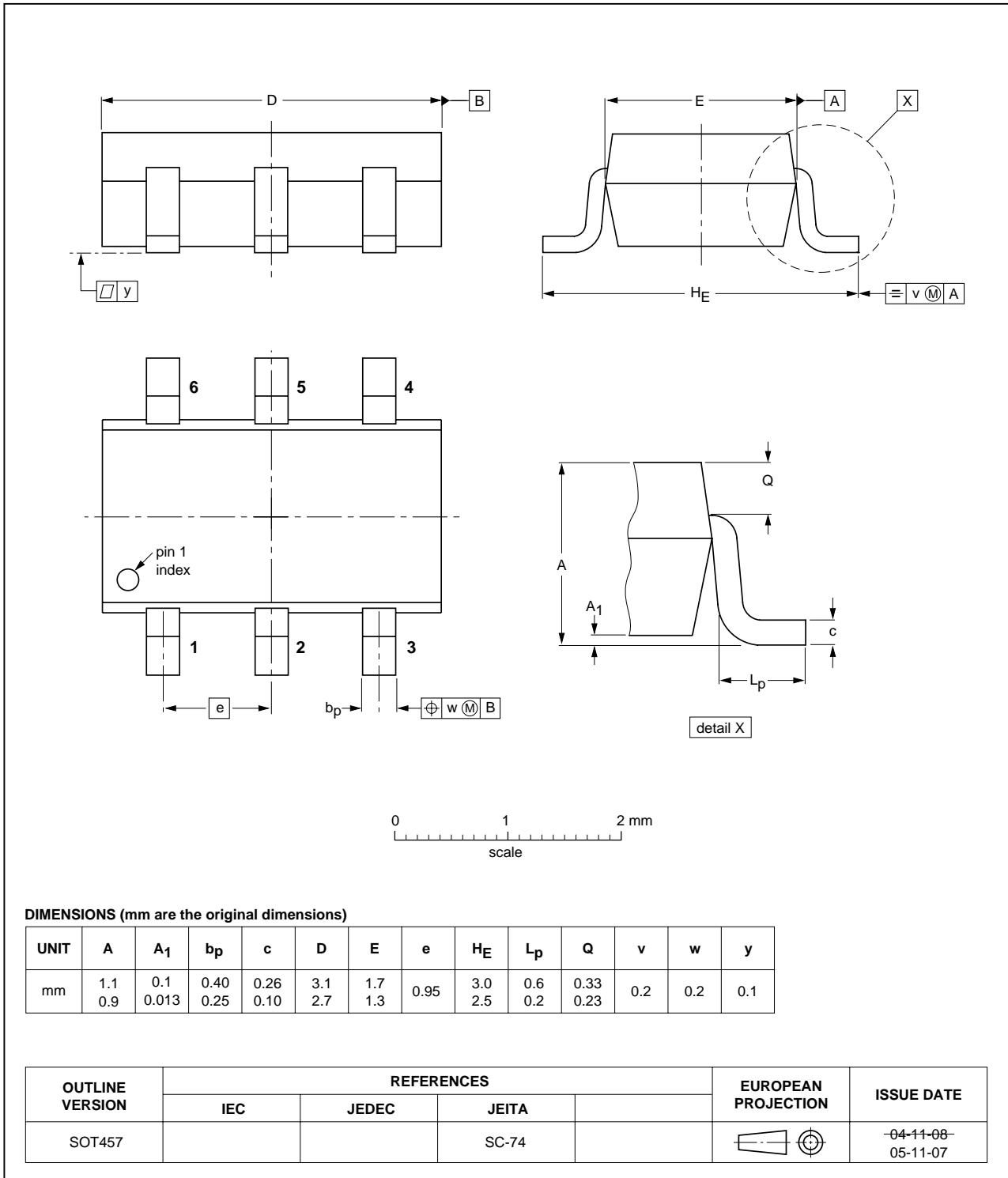


Fig 15. Package outline SOT457 (TSOP6)



8. Revision history

Table 6: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
PMN38EN_1	20060113	Product data sheet	-	-	-

9. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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