

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC7WT125FU

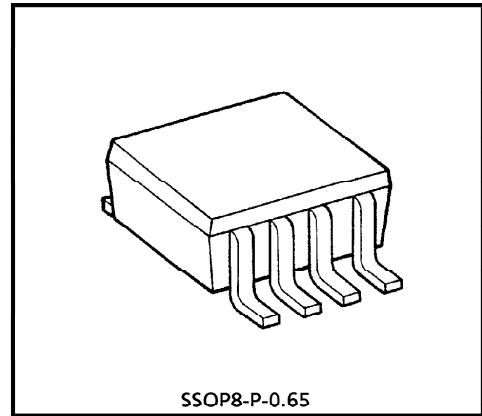
DUAL BUS BUFFER

The TC7WT125FU is a high speed CMOS DUAL BUS BUFFERS fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The input threshold levels are compatible with TTL output voltage.

The require 3-state control input \bar{G} to be set high to place the output into the high impedance.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.



Weight : 0.02g (Typ.)

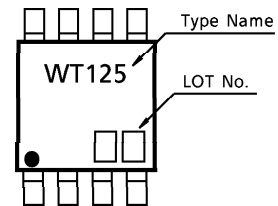
FEATURES

- High Speed $t_{pd} = 13ns$ (Typ.) at $V_{CC} = 5V$
- Low Power Dissipation $I_{CC} = 2\mu A$ (Max.) at $T_a = 25^\circ C$
- Compatible with TTL outputs ... $V_{IL} = 0.8V$ (Max.), $V_{IH} = 2.0V$ (Min.)
- Output Drive Capability 15 LSTTL Loads
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 6mA$ (Min.)

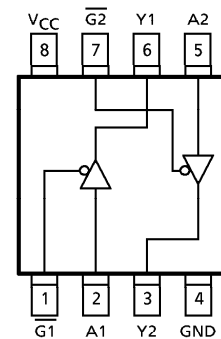
MAXIMUM RATINGS ($T_a = 25^\circ C$)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage Range	V_{CC}	-0.5~7	V
DC Input Voltage	V_{IN}	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 35	mA
DC V_{CC} / Ground Current	I_{CC}	± 37.5	mA
Power Dissipation	P_D	300	mW
Storage Temperature	T_{stg}	-65~150	$^\circ C$
Lead Temperature (10 s)	T_L	260	$^\circ C$

MARKING



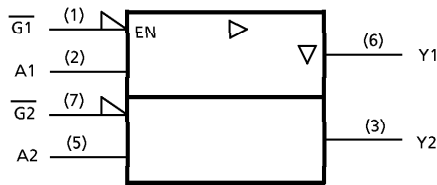
PIN ASSIGNMENT (TOP VIEW)



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LOGIC DIAGRAM



TRUTH TABLE

INPUTS		OUTPUTS
\overline{G}	A	Y
H	x	Z
L	L	L
L	H	H

x : Don't Care
Z : High Impedance

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	t_r, t_f	0~500	ns

DC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40\sim 85^\circ\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V_{IH}		4.5~5.5	2.0	—	—	2.0	—	V	
Low-Level Input Voltage	V_{IL}		4.5~5.5	—	—	0.8	—	0.8	V	
High-Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20\mu\text{A}$	4.5	4.4	4.5	—	4.4	—	V
			$I_{OH} = -6\text{mA}$	4.5	4.18	4.31	—	4.13	—	
Low-Level Output Voltage	V_{OL}	$V_{IN} = V_{IL}$	$I_{OL} = 20\mu\text{A}$	4.5	—	0.0	0.10	—	0.10	V
			$I_{OL} = 6\text{mA}$	4.5	—	0.17	0.26	—	0.33	
3-State Output Off-State Current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	5.5	—	—	± 0.5	—	± 5.0	μA	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	± 0.1	—	± 1.0	μA	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	2.0	—	20.0	μA	
	I_{CCT}	PER INPUT : $V_{IN} = 0.5\text{V}$ or 2.4V OTHER INPUT: V_{CC} or GND	5.5	—	—	2.0	—	2.9	mA	

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 6\text{ns}$)

CHARACTERISTIC	SYMBOL	TEST CONDITION	Ta = 25°C			Ta = -40~85°C		UNIT				
			C _L	V _{CC}	MIN.	TYP.	MAX.		MIN.	MAX.		
Output Transition Time	t _{TLH}	—	50	4.5	—	7	12	—	15	ns		
	t _{THL}			5.5	—	6	11	—	14			
Propagation Delay Time	t _{pLH}	—	50	4.5	—	15	25	—	31	ns		
				5.5	—	13	22	—	28			
	t _{pHL}		150	4.5	—	21	33	—	41			
				5.5	—	18	29	—	37			
Output Enable Time	t _{pZL}	R _L = 1kΩ	50	4.5	—	17	30	—	38	ns		
				5.5	—	14	27	—	34			
	t _{pZH}		150	4.5	—	23	38	—	48			
				5.5	—	20	34	—	43			
Output Disable Time	t _{pLZ}	R _L = 1kΩ	50	4.5	—	16	30	—	38	ns		
				5.5	—	13	27	—	34			
Input Capacitance	C _{IN}		—	—	—	—	5	10	—		10	pF
							Output Capacitance	C _{OUT}	—		—	
Power Dissipation Capacitance	C _{PD}	(Note 1)	—	—	—	32	—	—	—	pF		

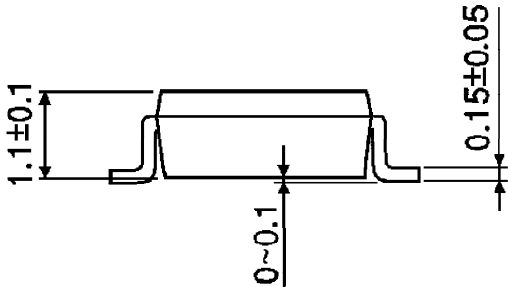
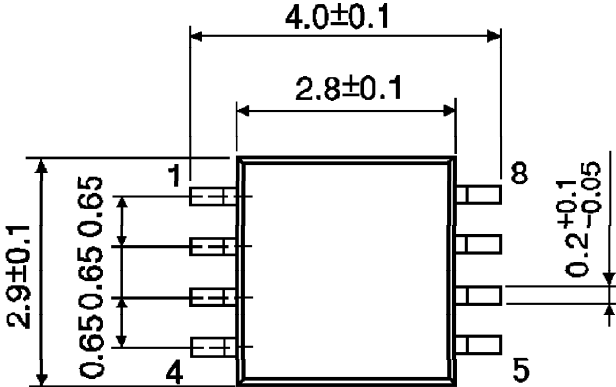
(Note 1) : C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \text{ (per Gate)}$$

OUTLINE DRAWING
SSOP8-P-0.65

Unit : mm



Weight : 0.02g (Typ.)