

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

## SSM3K15FV

High Speed Switching Applications

Analog Switch Applications

Optimum for high-density mounting in small packages

- Low on-resistance
  - :  $R_{on} = 4.0 \Omega$  (max) (@ $V_{GS} = 4 V$ )
  - :  $R_{on} = 7.0 \Omega$  (max) (@ $V_{GS} = 2.5 V$ )

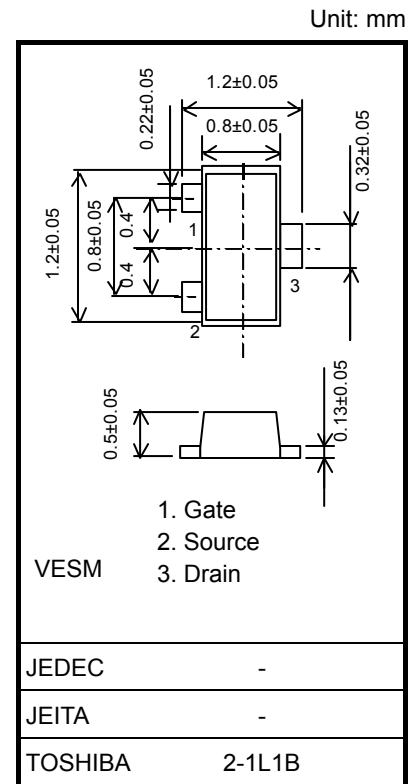
### Absolute Maximum Ratings ( $T_a = 25^\circ C$ )

Characteristics	Symbol	Rating	Unit
Drain-source voltage	$V_{DS}$	30	V
Gate-source voltage	$V_{GS}$	$\pm 20$	V
Drain current	DC	$I_D$	100
	Pulse	$I_{DP}$	200
Drain power dissipation ( $T_a = 25^\circ C$ )	$P_D$ (Note 1)	150	mW
Channel temperature	$T_{ch}$	150	$^\circ C$
Storage temperature	$T_{stg}$	-55~150	$^\circ C$

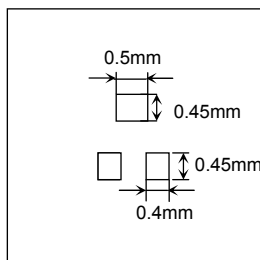
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

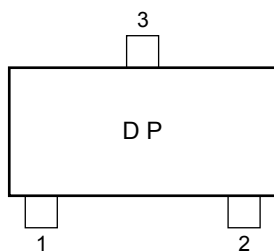
Note 1: Total rating, mounted on FR4 board (25.4 mm × 25.4 mm × 1.6 t)



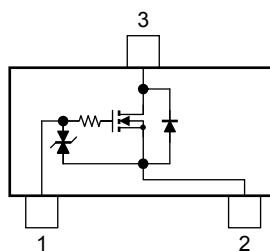
Weight: 0.0015 g (typ.)



### Marking



### Equivalent Circuit



### Handling Precaution

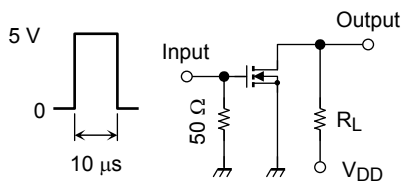
When handling individual devices (which are not yet mounted on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

## Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	$I_{GSS}$	$V_{GS} = \pm 16\text{ V}, V_{DS} = 0$	—	—	$\pm 1$	$\mu\text{A}$
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = 0.1\text{ mA}, V_{GS} = 0$	30	—	—	V
Drain cut-off current	$I_{DSS}$	$V_{DS} = 30\text{ V}, V_{GS} = 0$	—	—	1	$\mu\text{A}$
Gate threshold voltage	$V_{th}$	$V_{DS} = 3\text{ V}, I_D = 0.1\text{ mA}$	0.8	—	1.5	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 3\text{ V}, I_D = 10\text{ mA}$	25	—	—	mS
Drain-Source on-resistance	$R_{DS(ON)}$	$I_D = 10\text{ mA}, V_{GS} = 4\text{ V}$	—	2.2	4.0	$\Omega$
		$I_D = 10\text{ mA}, V_{GS} = 2.5\text{ V}$	—	4.0	7.0	
Input capacitance	$C_{iss}$	$V_{DS} = 3\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	7.8	—	pF
Reverse transfer capacitance	$C_{rss}$	$V_{DS} = 3\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	3.6	—	pF
Output capacitance	$C_{oss}$	$V_{DS} = 3\text{ V}, V_{GS} = 0, f = 1\text{ MHz}$	—	8.8	—	pF
Switching time	Turn-on time	$V_{DD} = 5\text{ V}, I_D = 10\text{ mA},$ $V_{GS} = 0 \sim 5\text{ V}$	—	50	—	ns
	Turn-off time		—	180	—	

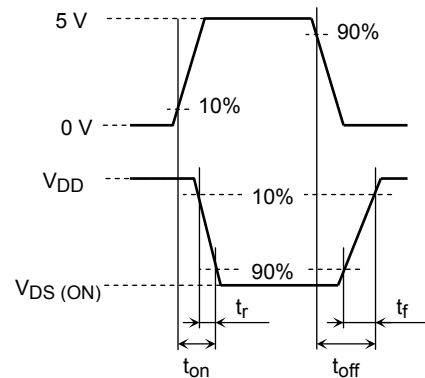
## Switching Time Test Circuit

(a) Test circuit



$V_{DD} = 5\text{ V}$   
 D.U.  $\leq 1\%$   
 Input:  $t_r, t_f < 5\text{ ns}$   
 $(Z_{out} = 50\ \Omega)$   
 Common Source  
 $T_a = 25^\circ\text{C}$

(b)  $V_{IN}$



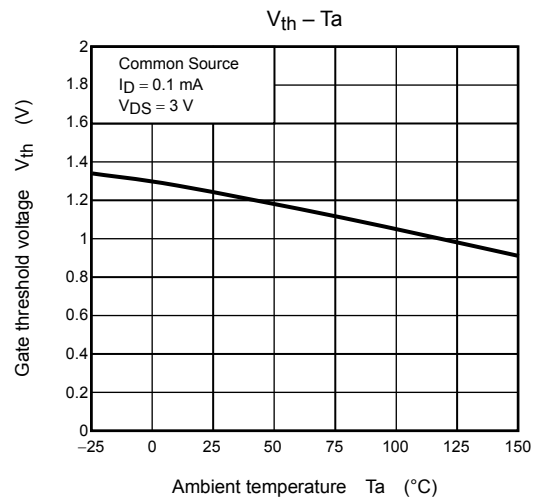
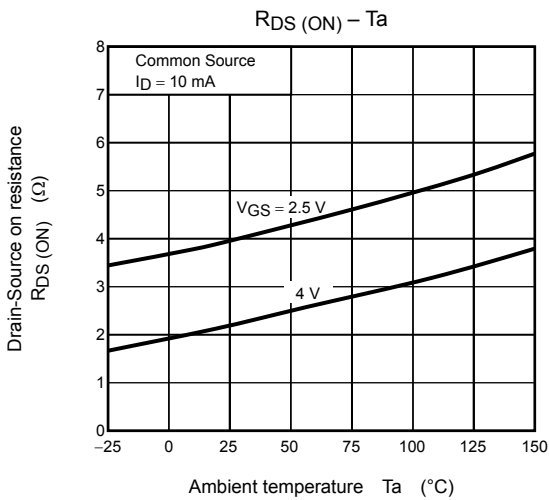
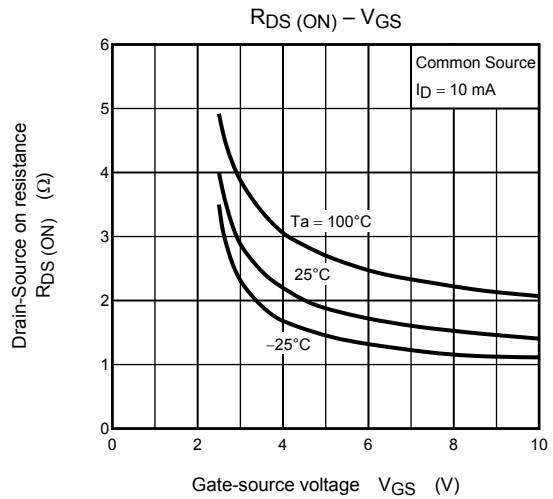
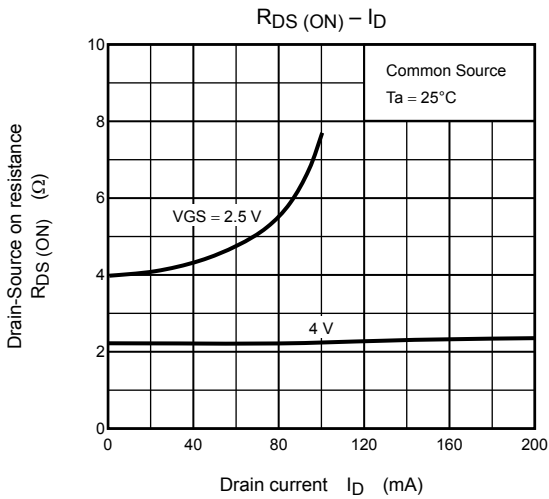
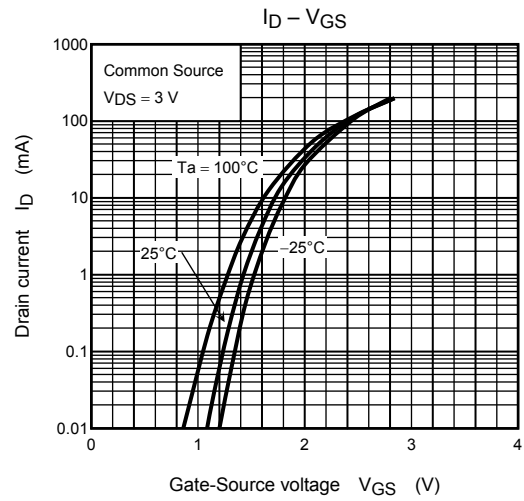
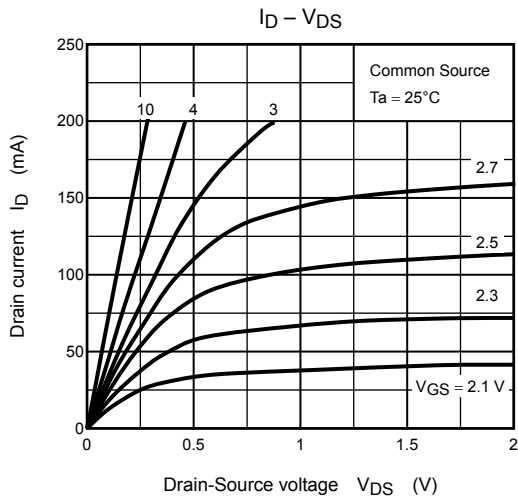
(c)  $V_{OUT}$

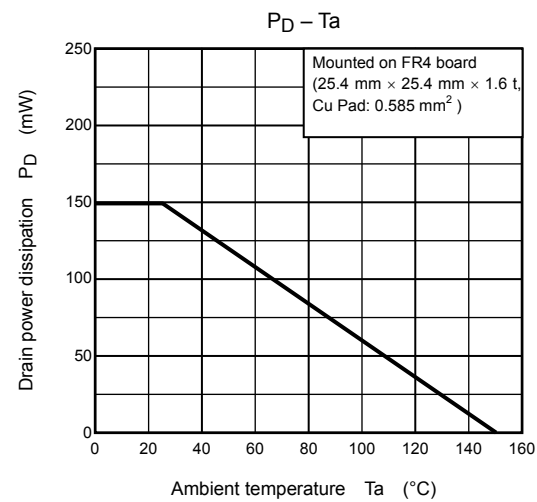
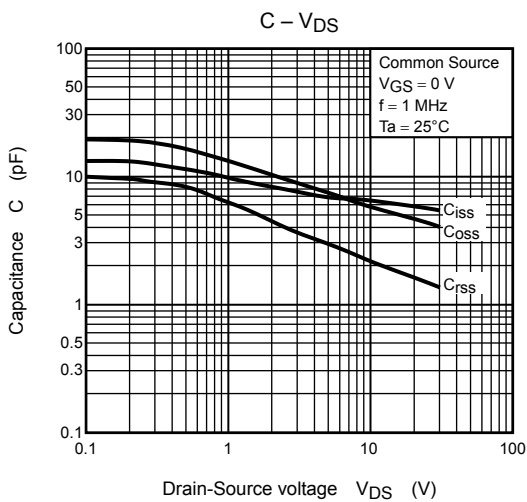
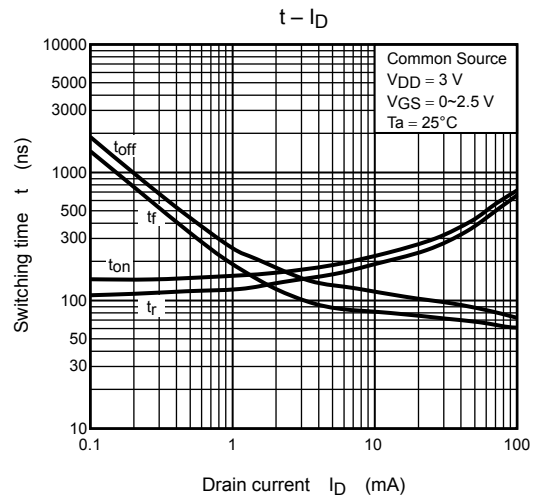
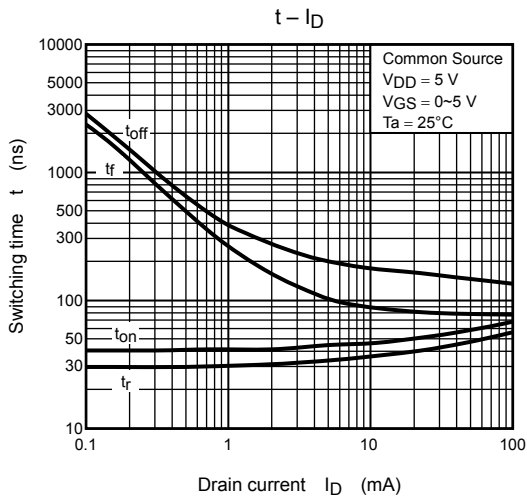
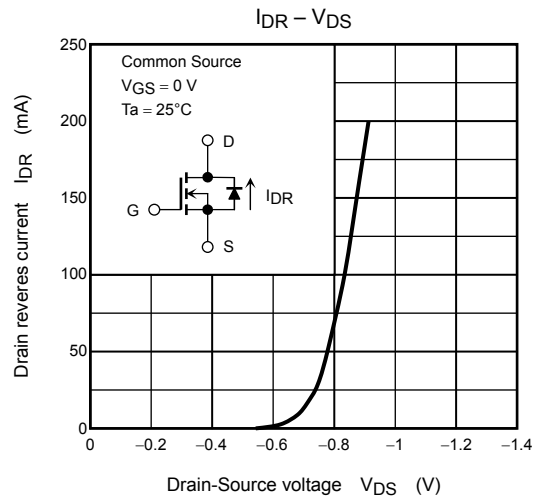
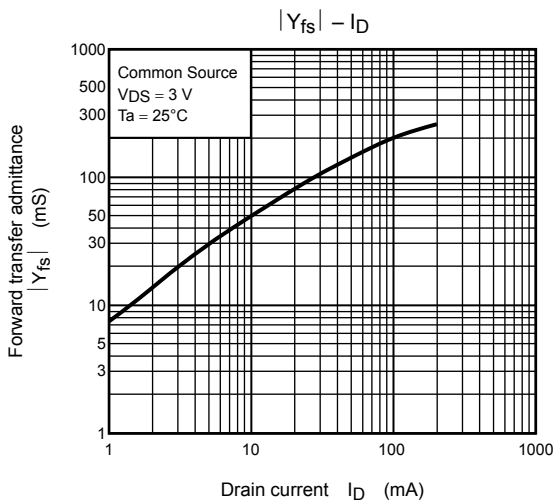
## Precaution

$V_{th}$  can be expressed as the voltage between gate and source when the low operating current value is  $I_D = 100\ \mu\text{A}$  for this product. For normal switching operation,  $V_{GS(on)}$  requires a higher voltage than  $V_{th}$  and  $V_{GS(off)}$  requires a lower voltage than  $V_{th}$ .

(The relationship can be established as follows:  $V_{GS(off)} < V_{th} < V_{GS(on)}$  )

Please take this into consideration when using the device.





**RESTRICTIONS ON PRODUCT USE**

20070701-EN GENERAL

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