

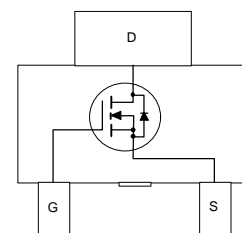
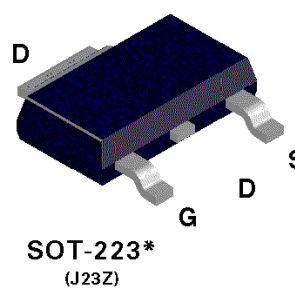
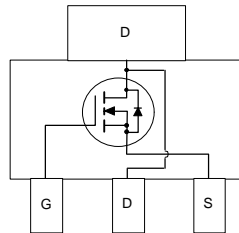
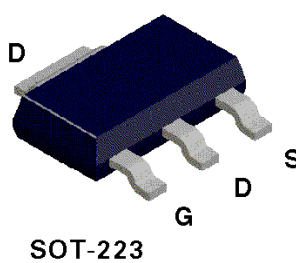
NDT453N N-Channel Enhancement Mode Field Effect Transistor

General Description

Power SOT N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 8A, 30V. $R_{DS(ON)} = 0.028\Omega$ @ $V_{GS} = 10V$.
 $R_{DS(ON)} = 0.042\Omega$ @ $V_{GS} = 4.5V$.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise not

Symbol	Parameter		NDT453N	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous	(Note 1a)	± 8	A
	- Pulsed		± 15	
P_D	Maximum Power Dissipation	(Note 1a)	3	W
		(Note 1b)	1.3	
		(Note 1c)	1.1	
T_J, T_{STG}	Operating and Storage Temperature Range		-65 to 150	$^\circ\text{C}$
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	42	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	12	$^\circ\text{C}/\text{W}$

* Order option J23Z for cropped center drain lead.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $T_J = 55^\circ\text{C}$			1	μA
					10	μA
I_{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ $T_J = 125^\circ\text{C}$	1	2	3	V
			0.7	1.5	2.2	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 8.0\text{ A}$ $T_J = 125^\circ\text{C}$ $V_{GS} = 4.5\text{ V}, I_D = 6.7\text{ A}$ $T_J = 125^\circ\text{C}$		0.022	0.028	Ω
				0.03	0.045	
				0.035	0.042	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$ $V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	15			A
			10			
g_{FS}	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 8.0\text{ A}$		14		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		890		pF
C_{oss}	Output Capacitance			560		pF
C_{rss}	Reverse Transfer Capacitance			190		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DD} = 25\text{ V}, I_D = 1\text{ A},$ $V_{GEN} = 10\text{ V}, R_{GEN} = 6\ \Omega$		10	15	ns
t_r	Turn - On Rise Time			20	35	ns
$t_{D(off)}$	Turn - Off Delay Time			40	50	ns
t_f	Turn - Off Fall Time			35	50	ns
Q_g	Total Gate Charge	$V_{DS} = 15\text{ V}, I_D = 8.0\text{ A}, V_{GS} = 10\text{ V}$		28	35	nC
Q_{gs}	Gate-Source Charge			4.5		nC
Q_{gd}	Gate-Drain Charge			9.5		nC

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				2.3	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 8.0\text{ A}$ (Note 2)		0.8	1.3	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}$, $I_S = 2\text{ A}$, $di_F/dt = 100\text{ A}/\mu\text{s}$			100	ns

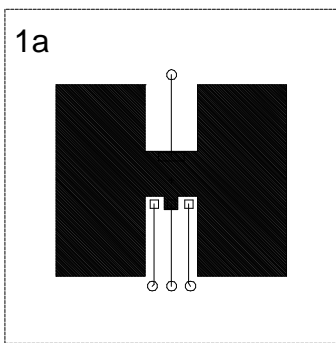
Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

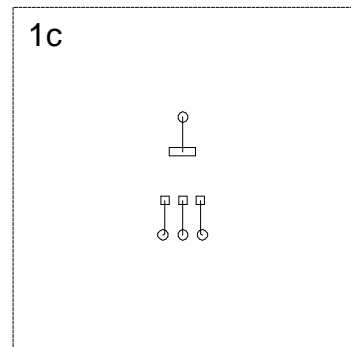
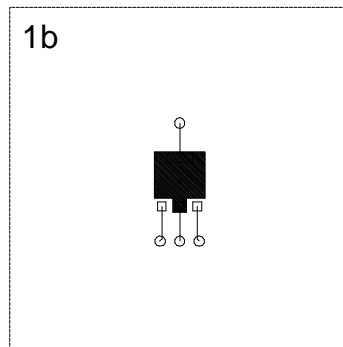
$$P_D(t) = \frac{T_J - T_A}{R_{\theta J \phi}(t)} = \frac{T_J - T_A}{R_{\theta J} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(on)} \theta_{TJ}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

- 42°C/W when mounted on a 1 in² pad of 2oz copper.
- 95°C/W when mounted on a 0.066 in² pad of 2oz copper.
- 110°C/W when mounted on a 0.0123 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper



- Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Typical Electrical Characteristics

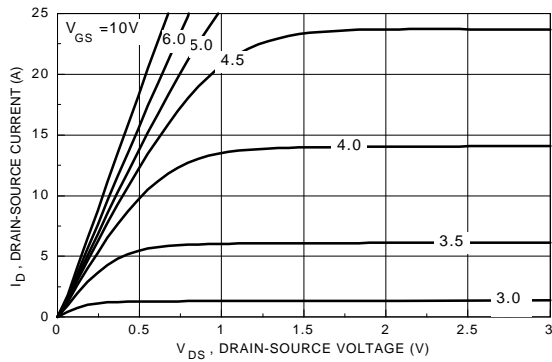


Figure 1. On-Region Characteristics.

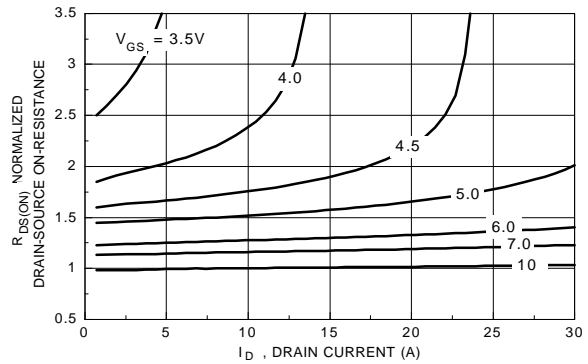


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

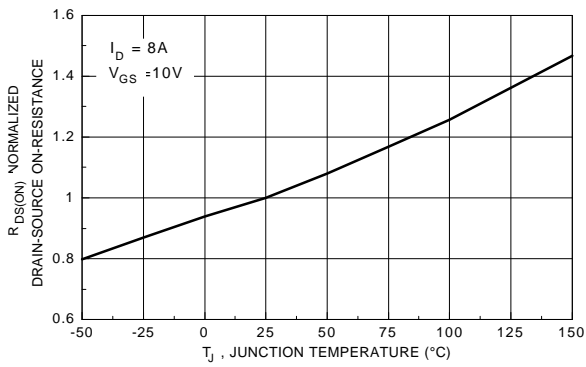


Figure 3. On-Resistance Variation with Temperature.

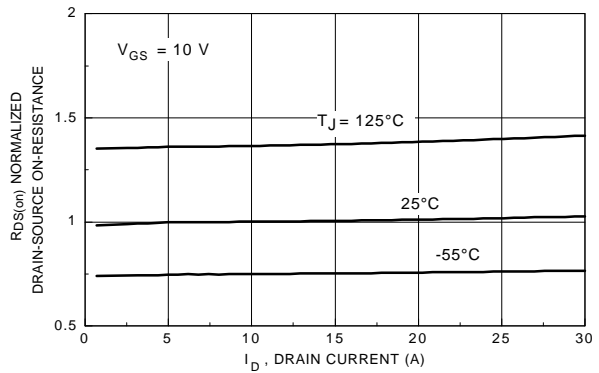


Figure 4. On-Resistance Variation with Drain Current and Temperature.

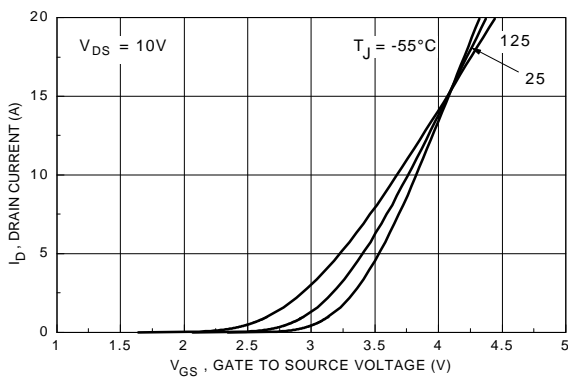


Figure 5. Transfer Characteristics.

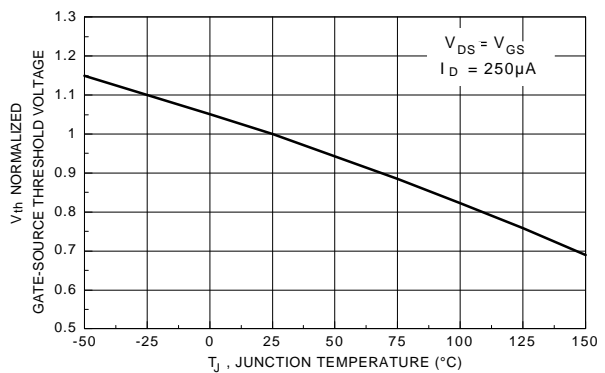


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

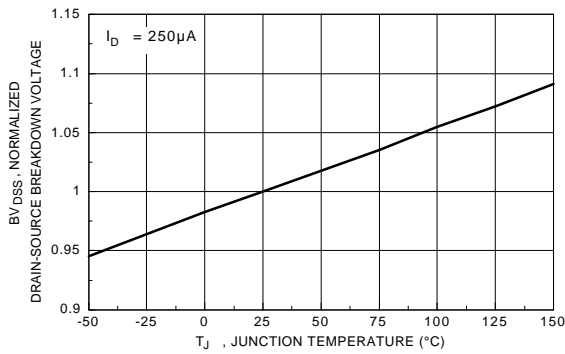


Figure 7. Breakdown Voltage Variation with Temperature.

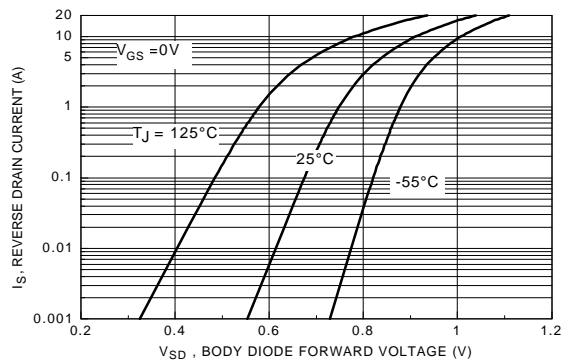


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

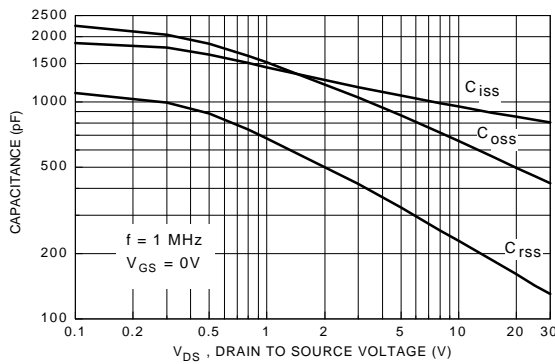


Figure 9. Capacitance Characteristics.

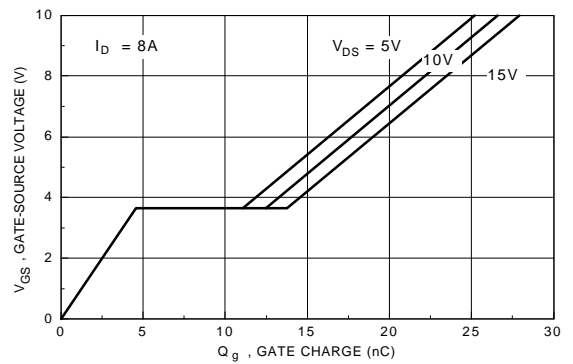


Figure 10. Gate Charge Characteristics.

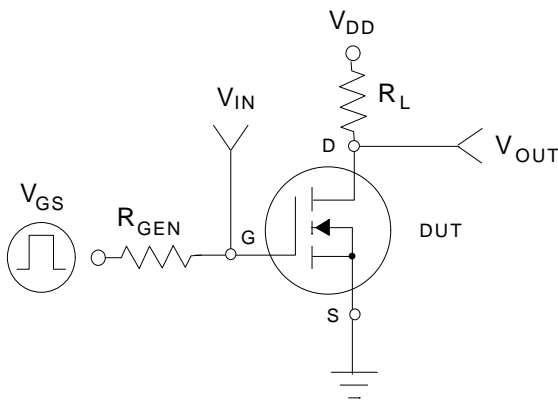


Figure 11. Switching Test Circuit.

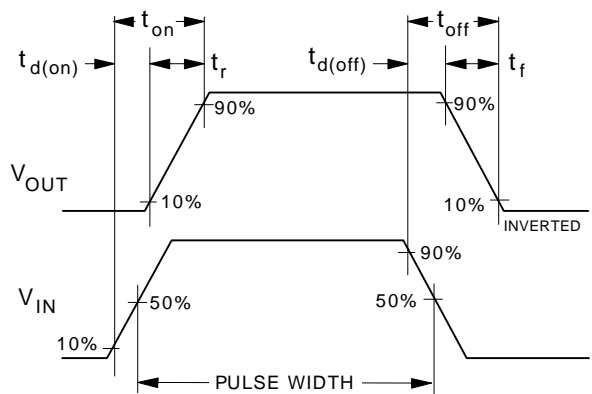


Figure 12. Switching Waveforms.

Typical Electrical and Thermal Characteristics

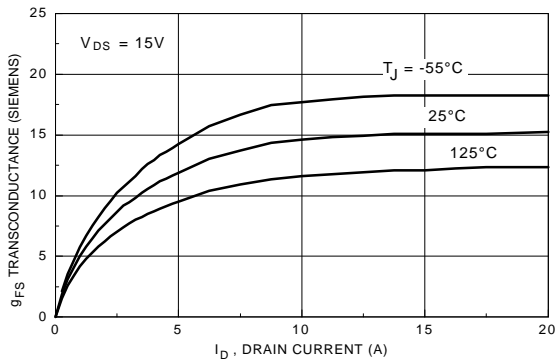


Figure 13. Transconductance Variation with Drain Current and Temperature.

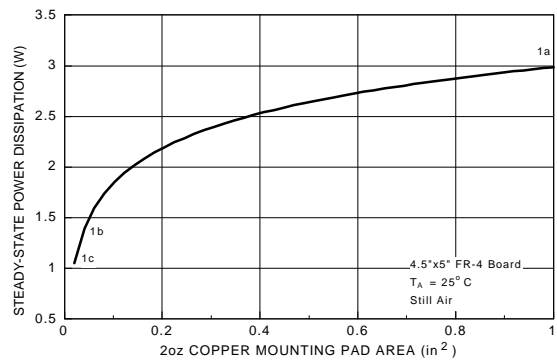


Figure 14. SOT-223 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

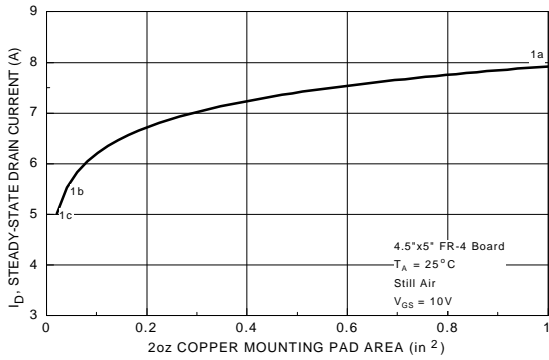


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

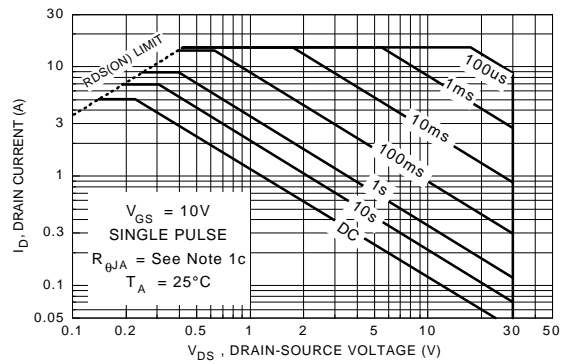


Figure 16. Maximum Safe Operating Area.

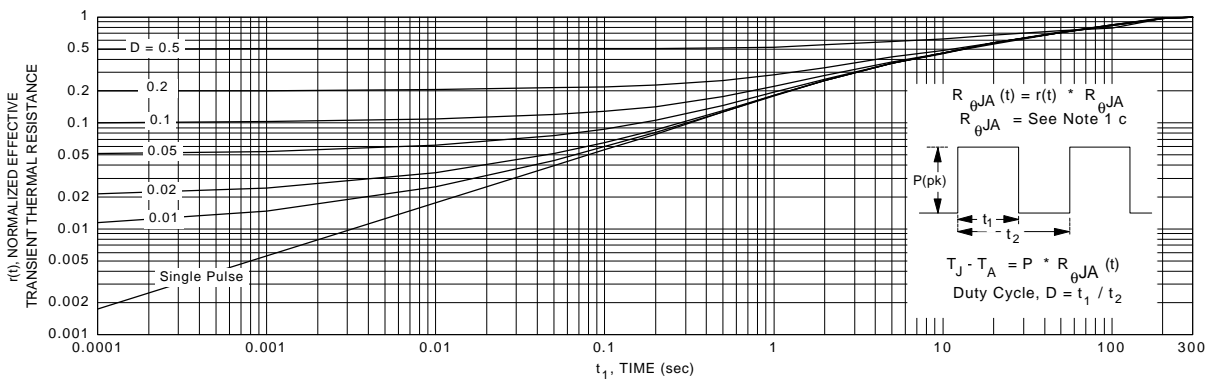


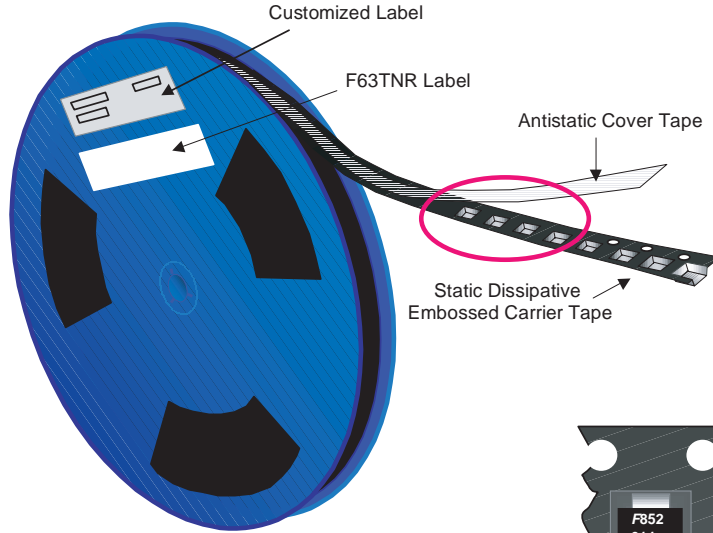
Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

SOT-223 Tape and Reel Data and Package Dimensions

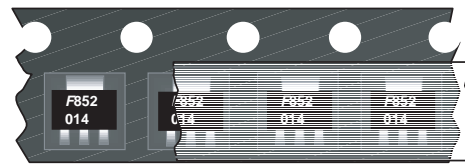


SOT-223 Packaging Configuration: Figure 1.0

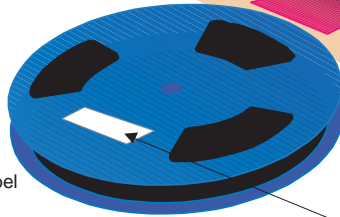
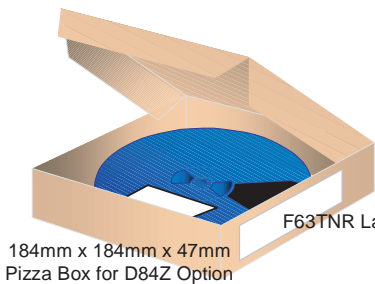
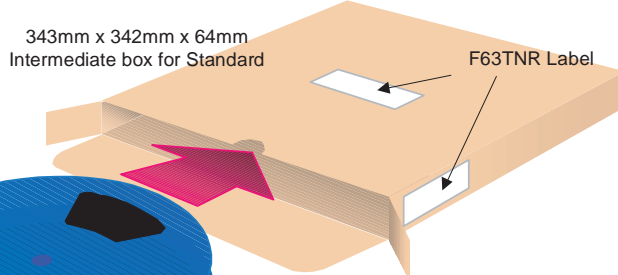


Packaging Description:
 SOT-223 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13" or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 500 units per 7" or 177cm diameter reel. This and some other options are further described in the Packaging Information table.
 These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.

SOT-223 Packaging Information		
Packaging Option	Standard (no flow code)	D84Z
Packaging type	TNR	TNR
Qty per Reel/Tube/Bag	2,500	500
Reel Size	13" Dia	7" Dia
Box Dimension (mm)	343x64x343	184x187x47
Max qty per Box	5,000	1,000
Weight per unit (gm)	0.1246	0.1246
Weight per Reel (kg)	0.7250	0.1532
Note/Comments		



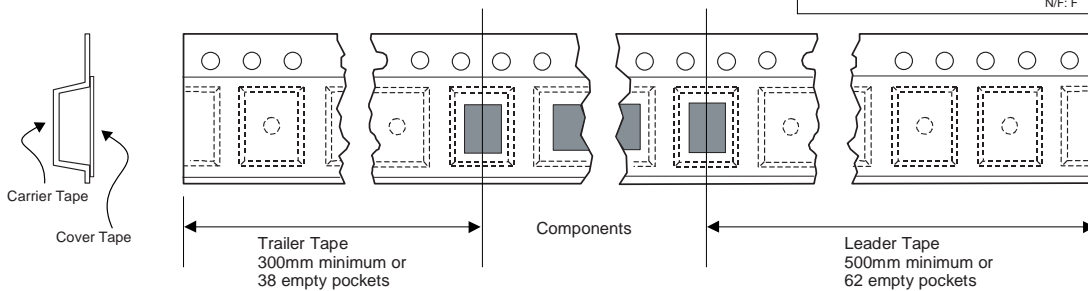
SOT-223 Unit Orientation



F63TNR Label sample

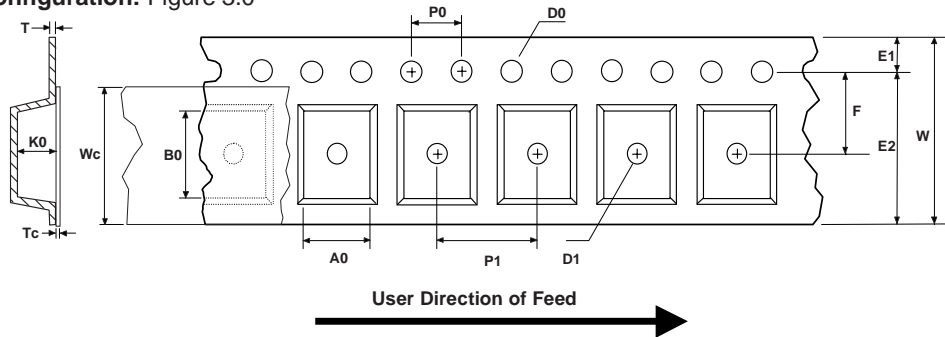
LOT: CBVK741B019	QTY: 3000
FSID: PN2222A	SPEC:
D/C1: D984Z	QTY1:
D/C2:	QTY2:
SPEC REV:	CPN:
	N/F: F
	(F63TNR)3

SOT-223 Tape Leader and Trailer Configuration: Figure 2.0



SOT-223 Tape and Reel Data and Package Dimensions, continued

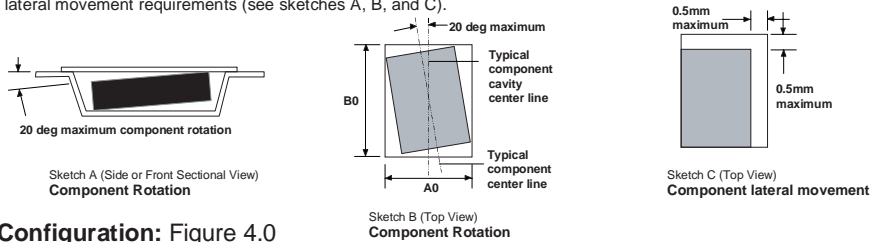
SOT-223 Embossed Carrier Tape Configuration: Figure 3.0



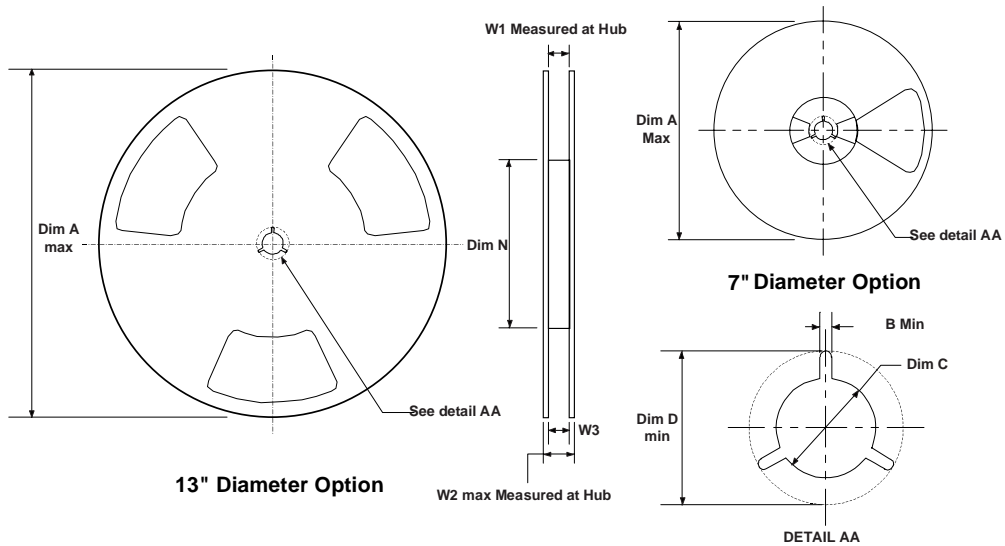
Dimensions are in millimeter

Pkg type	A0	B0	W	D0	D1	E1	E2	F	P1	P0	K0	T	Wc	Tc
SOT-223 (12mm)	6.83 +/-0.10	7.42 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.50 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	1.88 +/-0.10	0.292 +/- 0.0130	9.5 +/-0.025	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



SOT-223 Reel Configuration: Figure 4.0



Dimensions are in inches and millimeters

Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	5.906 150	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4

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E ² CMOS™	PowerTrench™	
FACT™	QFET™	
FACT Quiet Series™	QS™	
FAST®	Quiet Series™	
FASTr™	SuperSOT™-3	
GTO™	SuperSOT™-6	
HiSeC™	SuperSOT™-8	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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