Ordering number : ENN7298

N-Channel and P-Channel Silicon MOSFETs

FW351

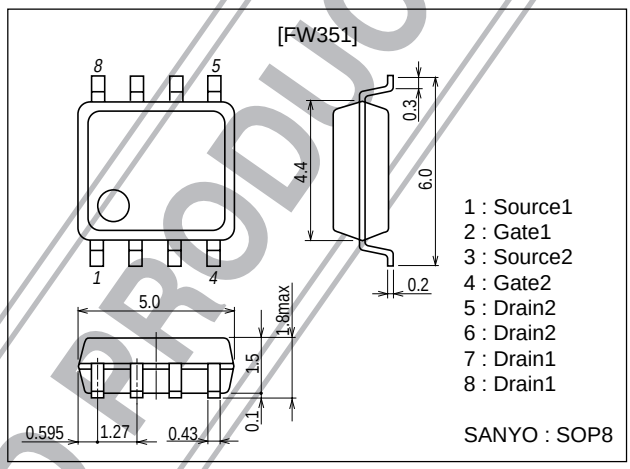
Ultrahigh-Speed Switching Applications

Features

- N-channel and P-channel MOSFETs featuring low ON-resistance, high-speed switching, and 4V voltage operation are encapsulated in one package to enable high-density mounting.
- Low ON-resistance.

Package Dimensions

unit : mm
2129



Specifications

Absolute Maximum Ratings at Ta=25°C

Parameter	Symbol	Conditions	Ratings		Unit
			N-channel	P-channel	
Drain-to-Source Voltage	V_{DSS}		60	−60	V
Gate-to-Source Voltage	V_{GSS}		±20	±20	V
Drain Current (DC)	I_D		5	−3	A
Drain Current (Pulse)	I_{DP}	PW≤10μs, duty cycle≤1%	52	−32	A
Allowable Power Dissipation	P_D	Mounted on a ceramic board (1200mm²×0.8mm)1unit	1.7		W
Total Dissipation	P_T	Mounted on a ceramic board (1200mm²×0.8mm)	2.0		W
Channel Temperature	Tch		150		°C
Storage Temperature	Tstg		−55 to +150		°C

Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[N-channel]						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=1mA, V_{GS}=0	60			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V, V_{GS}=0			10	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0			±10	μA
Cutoff Voltage	$V_{GS(off)}$	V_{DS}=10V, I_D=1mA	1.0		2.4	V
Forward Transfer Admittance	$\|yfs\|$	V_{DS}=10V, I_D=5A	7	10		S

Marking : W351

Continued on next page.

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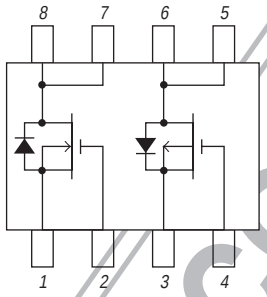
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Static Drain-to-Source On-State Resistance	$R_{DS}(on)1$	I_D=5A, V_{GS}=10V		44	57	mΩ
	$R_{DS}(on)2$	I_D=3A, V_{GS}=4V		58	81	mΩ
Input Capacitance	Ciss	V_{DS}=20V, f=1MHz		550		pF
Output Capacitance	Coss	V_{DS}=20V, f=1MHz		170		pF
Reverse Transfer Capacitance	Crss	V_{DS}=20V, f=1MHz		60		pF
Turn-ON Delay Time	$t_d(on)$	See specified Test Circuit.		11		ns
Rise Time	t_r	See specified Test Circuit.		50		ns
Turn-OFF Delay Time	$t_d(off)$	See specified Test Circuit.		65		ns
Fall Time	t_f	See specified Test Circuit.		70		ns
Total Gate Charge	Qg	V_{DS}=10V, V_{GS}=10V, I_D=5A		19		nC
Gate-to-Source Charge	Qgs	V_{DS}=10V, V_{GS}=10V, I_D=5A		3		nC
Gate-to-Drain “Miller” Charge	Qgd	V_{DS}=10V, V_{GS}=10V, I_D=5A		4.2		nC
Diode Forward Voltage	V_{SD}	I_S=5A, V_{GS}=0		0.8	1.2	V
[P-channel]						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=–1mA, V_{GS}=0	–60			V
Zero-Gate Voltage Drain Current	I_{DSS}	V_{DS}=–60V, V_{GS}=0			–10	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±16V, V_{DS}=0			±10	μA
Cutoff Voltage	V_{GS}(off)	V_{DS}=–10V, I_D=–1mA	–1.0		–2.4	V
Forward Transfer Admittance	|yfs|	V_{DS}=–10V, I_D=–3A	4.5	6.3		S
Static Drain-to-Source On-State Resistance	$R_{DS}(on)1$	I_D=–3A, V_{GS}=–10V		105	140	mΩ
	$R_{DS}(on)2$	I_D=–1.5A, V_{GS}=–4V		150	210	mΩ
Input Capacitance	Ciss	V_{DS}=–20V, f=1MHz		680		pF
Output Capacitance	Coss	V_{DS}=–20V, f=1MHz		170		pF
Reverse Transfer Capacitance	Crss	V_{DS}=–20V, f=1MHz		50		pF
Turn-ON Delay Time	$t_d(on)$	See specified Test Circuit.		11		ns
Rise Time	t_r	See specified Test Circuit.		30		ns
Turn-OFF Delay Time	$t_d(off)$	See specified Test Circuit.		90		ns
Fall Time	t_f	See specified Test Circuit.		45		ns
Total Gate Charge	Qg	V_{DS}=–10V, V_{GS}=–10V, I_D=–3A		22		nC
Gate-to-Source Charge	Qgs	V_{DS}=–10V, V_{GS}=–10V, I_D=–3A		4		nC
Gate-to-Drain “Miller” Charge	Qgd	V_{DS}=–10V, V_{GS}=–10V, I_D=–3A		5		nC
Diode Forward Voltage	V_{SD}	I_S=–3A, V_{GS}=0		–0.8	–1.2	V

Electrical Connection

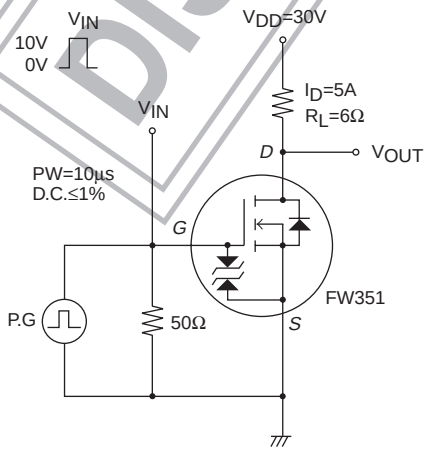


1 : Source1
2 : Gate1
3 : Source2
4 : Gate2
5 : Drain2
6 : Drain2
7 : Drain1
8 : Drain1

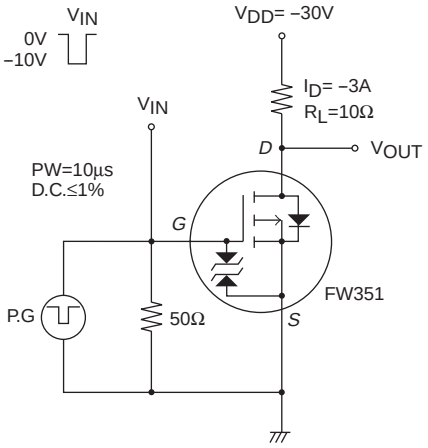
(Top view)

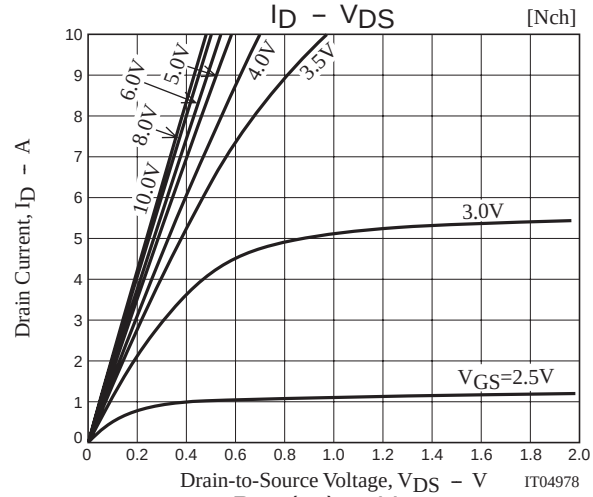
Switching Time Test Circuit

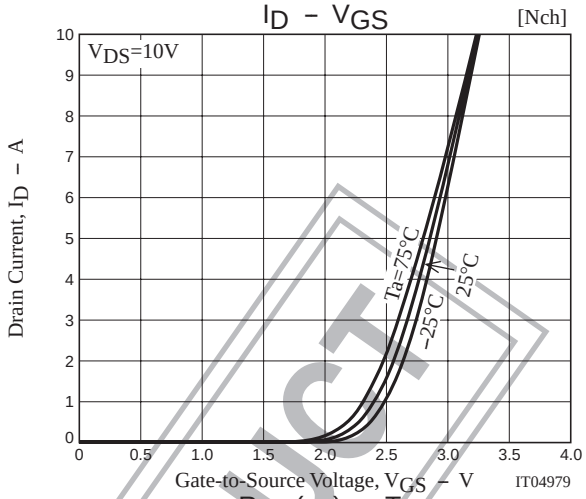
[N-channel]

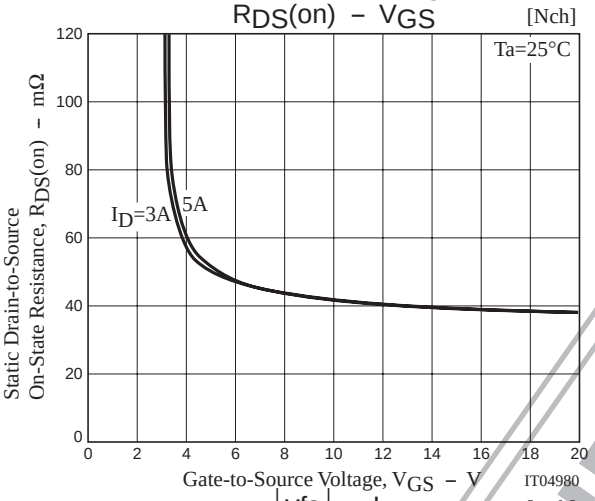


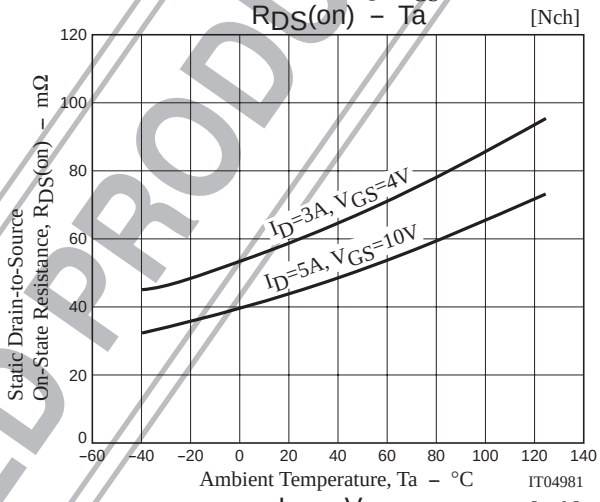
[P-channel]

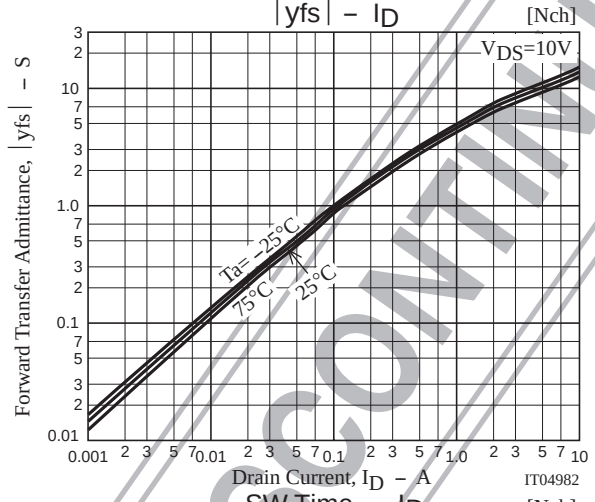


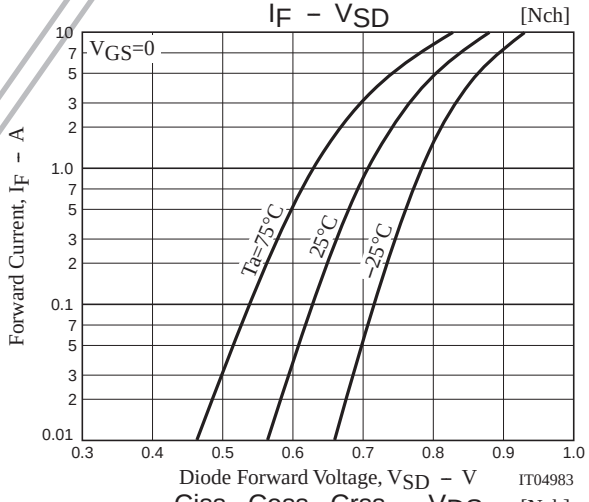


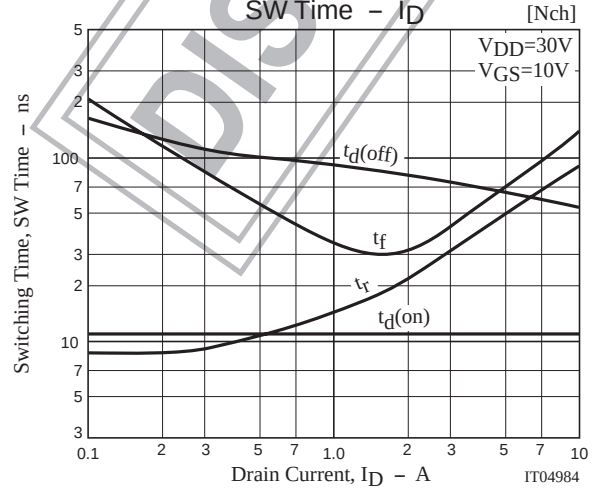


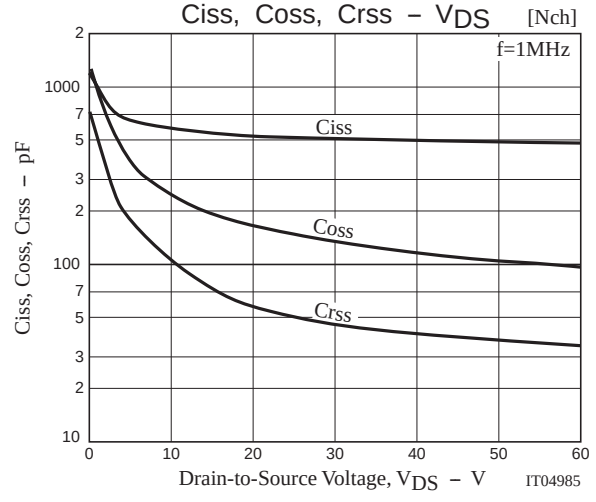


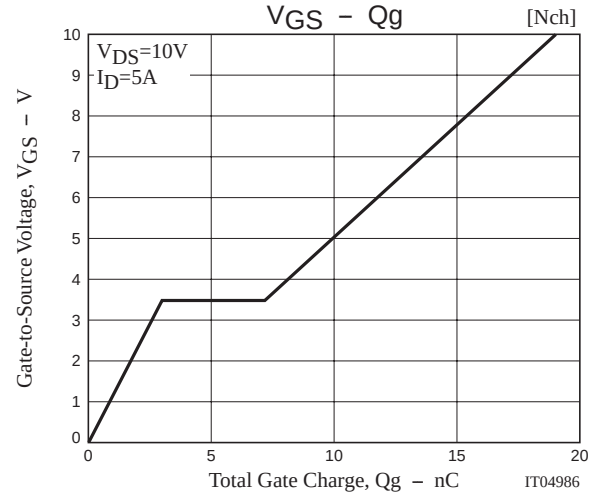


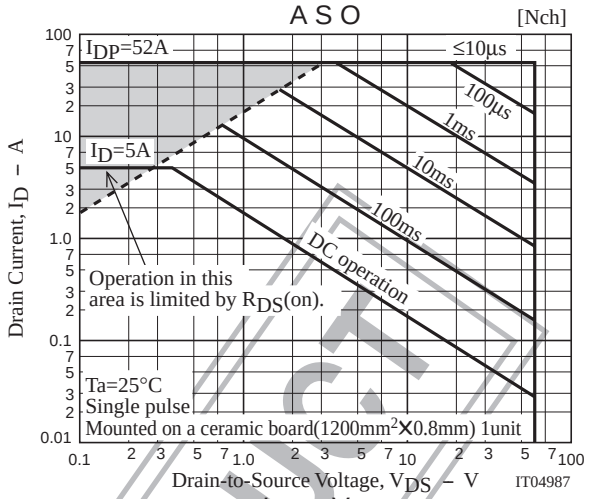


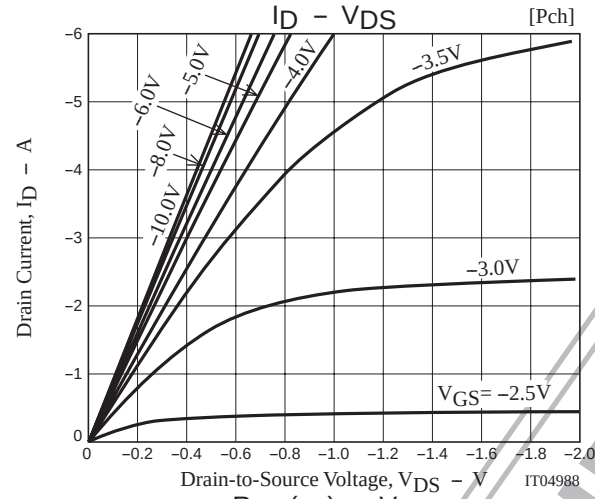


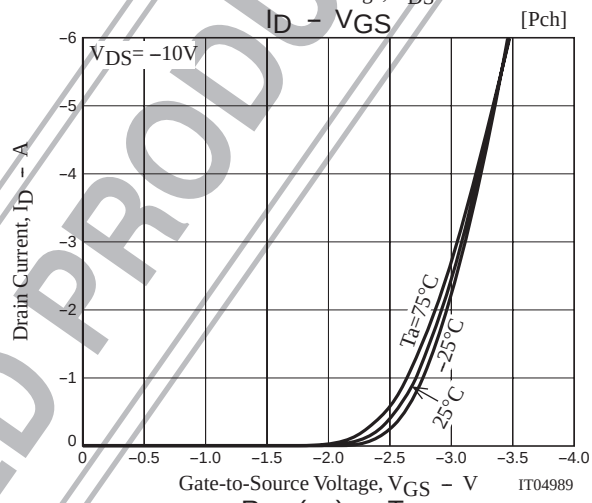


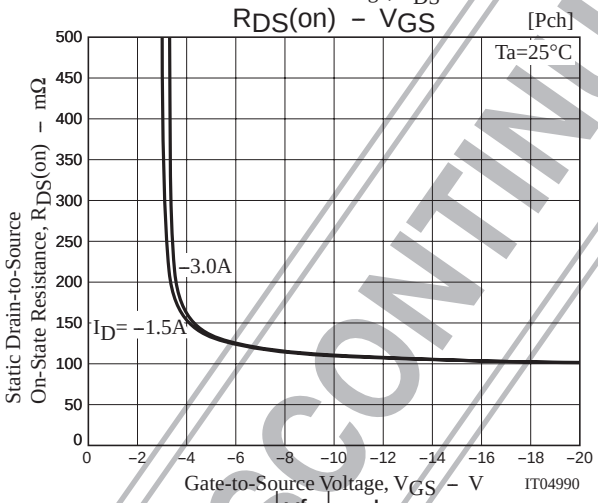


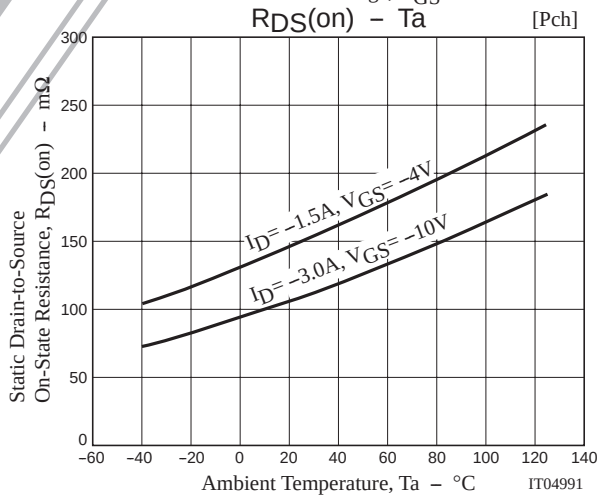


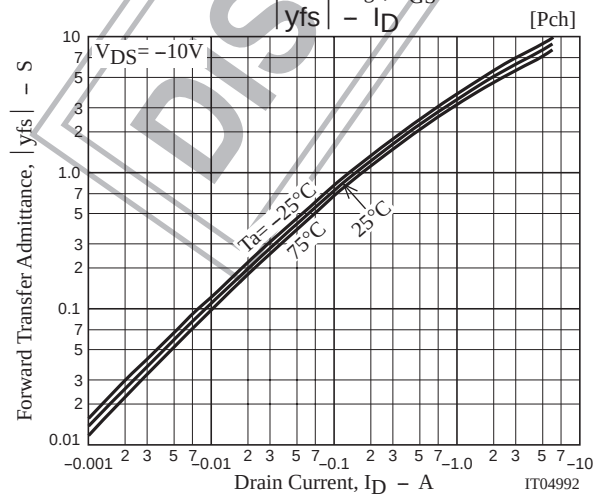


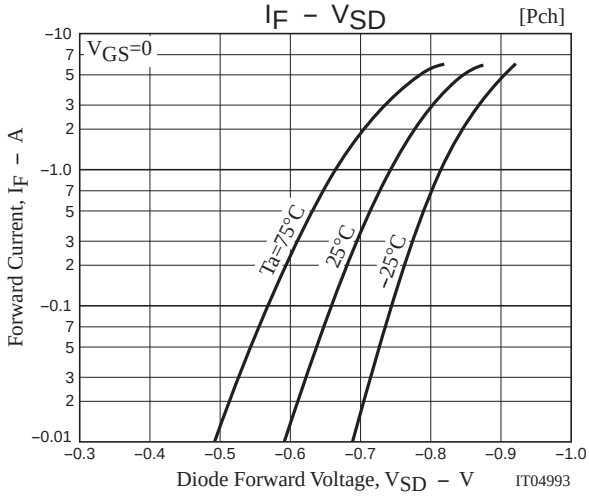




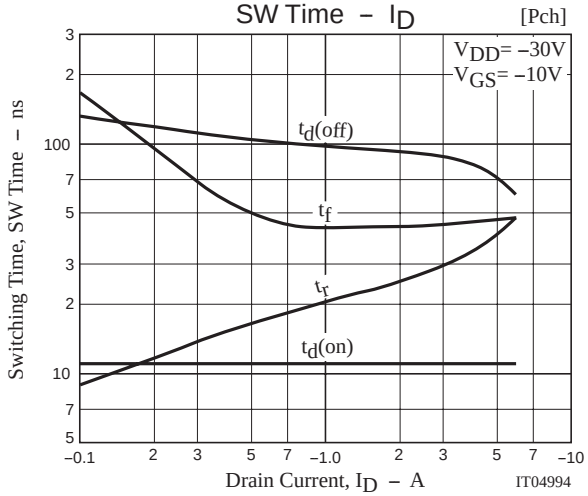




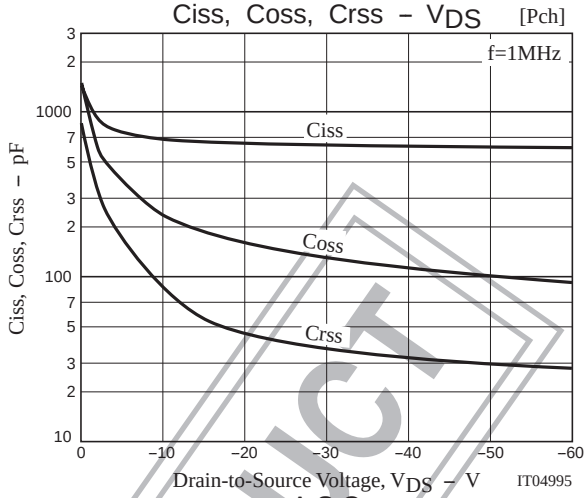




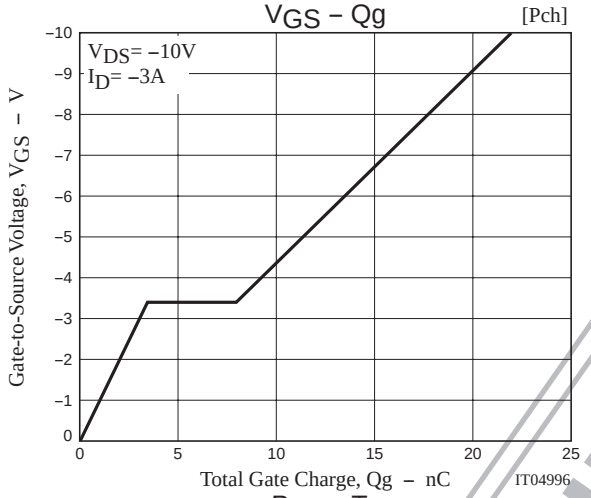
SW Time – I_D [Pch]



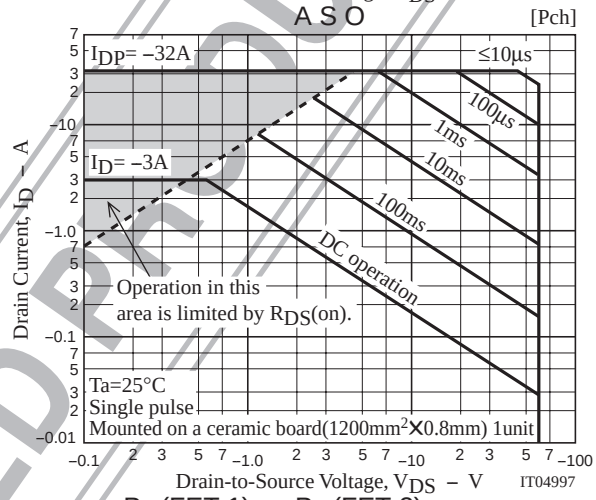
Ciss, Coss, Crss – V_{DS} [Pch]



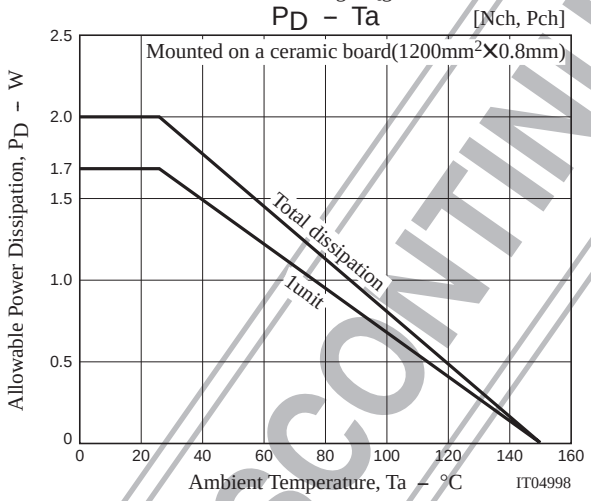
V_{GS} – Qg [Pch]



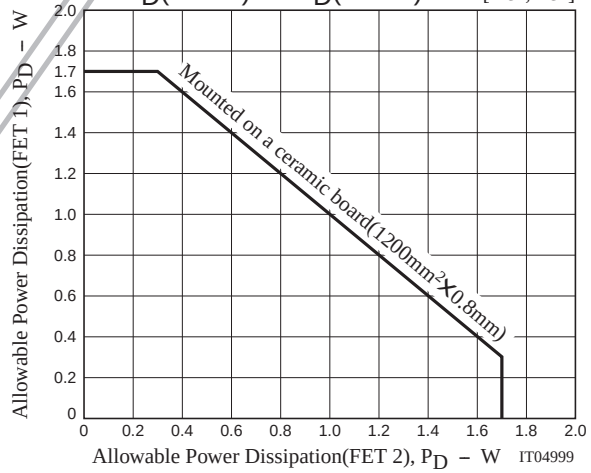
A S O [Pch]



P_D – Ta [Nch, Pch]



P_D(FET 1) – P_D(FET 2) [Nch, Pch]



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